Basics of Electronics

By

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Chapter-1
Semiconductor

Conductor , Semiconductor & Insulators

Conductors: Semiconductors are those materials whose electrical conductivity is vary high ,through these materials electricity pass easily .The valence band and the conduction band overlap each other i.e. their is no forbidden energy gap (E_g=0). At absolute zero temperature ,large number of electrons remain in the conduction band. for example : copper , alluminium , gold etc.

Semiconductors: Semiconductors are those materials whose electrical conductivity is between conductors and insulators. The forbidden energy gap of a semiconductor is nearly same as insulator. The energy gap is narrower. The value of E_g=1.1eV for silicon crystal and E_g=0.7eV for germanium at ok. It can easily overcome due to thermal agitation or light. A semiconductor remains partially full valence band and partially full conduction band at the room temperature.

Insulator: Through these materials electricity cannot pass .Plastic, glass, wood etc are the examples of insulators. The valence band of these material remains full of electrons & the conduction band of these material remains empty. The forbidden energy gap between is widest i.e. is more than 10ev.

Intrinsic Semiconductors

An intrinsic semiconductor is a pure semiconductors .When an external voltage is applied to the instrinsic semiconductor, the free electrons flow toward the +ve battery terminal and the holes flow toward the negative terminal.

Two types of flow

Two types of carrier flow exist in an intrinsic semiconductor. First, there is the flow of free electrons through larger orbits (conduction band). Second, there is the flow of holes through smaller orbits(valence band)

Doping a Semiconductor

Doping is the process of control addition of impurity in pure semi conductor, it increases the conductivity of a semiconductor. A doped semiconductor is called extrinsic semiconductor. When an intrinsic semiconductor is doped with pentavalent (doner) atoms, it has more free electrons then holes. When an intrinsic semiconductor is doped with trivalent (acceptor) atoms, it has more holes then free electrons.

Two types of extrinsic semiconductors

In an n-type semiconductor the free electrons are the majority carrier, and the holes are minority carriers. In a p-type semiconductor the holes are the majority carriers, and the free electrons are the minority carriers.

pn Junction

It is a border between p-type & n-type semiconductor. The pn- junction itself forms the most basic semiconductor device called semiconductor diode, thus semiconductor diode and pn junction are one and the same.

Depletion layer

In pn junction diode the the free electrons on n side tend to diffuse across the junction ,when free electrons enters the p region, the free electrons recombines with hole in p region, and due to which hole disappears and free electron becomes valence electron.

Each time an electron diffuses across a junction , it creates a pair of ions , +ve ion on n side and -ve ion on p side, these pair of ions at junction is called a dipole. As no. of dipoles builds up, empty charge region is created know as depletion region.

Junction Potential width of depletion layer

Width of depletion layer is the distance measured from one side to the other side of the depletion region. Due to the presence of depletion region the electrons and holes do not i.e. depletion region acts as a

barrier. Due to the presence of immobile +ve(n-side) and –ve (p-side) ions on opposite sides of the junction an electric field is created across the junction . This electric field is known as junction potential also known as barrier potential. The barrier potential for silicon is 0.7 volt whereas for germanium is 0.3 volt at 25^0C.

Forward bias & Reverse bias

When an external voltage opposes the barrier potential, the diode is forward biased. If the applied voltage is greater than the barrier potential, the current flows. When an external voltage opposes the barrier potential, the diode is forward biased.

Diffusion of carriers in semiconductor : -

The movement of charge carriers from the region of high carrier concentration to the areas of low concentration, recombination of charge carriers occurs, the process is known as diffusion of carriers. The rate at which diffusion occurs depends on the velocity at which carriers move and on the distance between the carriers.

This diffusion current is proportional to the concentration gradient :

$$J_{nd} = q.D_n.\frac{\partial n}{\partial x}$$

$$J_{pd} = -q.D_p.\frac{\partial p}{\partial x}$$

Where D_n and D_p are the diffusion constant of p and n- type semiconductor, generally free electrons moves in conduction band & holes in valence band , valence band is more effected by electrostatic force so , we say mobility(it is the ease with which charge carriers flow) of electrons is higher then that of holes .

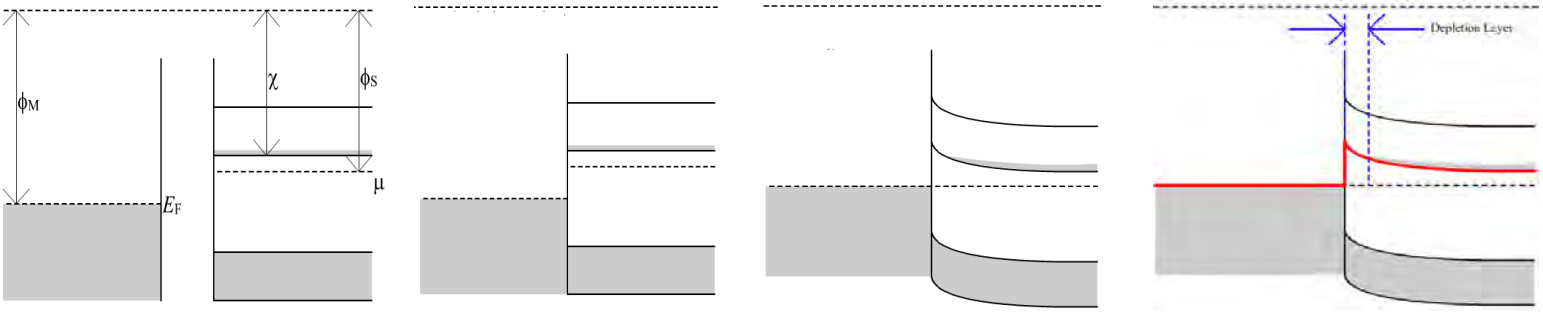
The mobility of electron being higher than that of holes, the Einstein relationship shows that, for a given concentration gradient, the diffusion current for electrons is higher than the diffusion current for holes.

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{q}$$

Work function in metals and semiconductor junction:-

Energy required for an electron to move from Fermi level into the free space known as work function .The schematic below in fig. a shows a metal and an *n*-type semiconductor. The dashed line at the top represents the zero of energy of free space.

In fig. a, the work functions of metal & semi conductor denoted by Φ_M & Φ_S resp., E_F & μ indicates the fermi level of metal & semi conductor resp, χ i.e. electron effinity.



(a) (b) (c) (d)

When contact is made as shown in fig. b, electrons lower their energy by flowing from the semiconductor conduction band into the metal. This continues until the fermi energy level in the semiconductor as shown in fig. c reaches equilibrium with the fermi energy of the metal. The deformed band structure as shown in fig. d known as depletion layer forms a potential barrier.

The Energy Hill

The barrier potential of a diode looks like an energy hill. Electrons attempting to cross the junction need to have enough energy to climb this hill. An external voltage source that forward-bais the diode gives electrons the energy required to pass through the depletion layer.

Barrier Potential & Temperature

When the junction temperature increases, the depletion layer becomes narrow & the barrier potential decreases. It will decrease . It will decrease approximately 2.5 mV for each ^{0}C increase.

Field and capacitance of depletion layer

The two types of capacitances associated with a p-n junction diode are

1. Transition capacitance (C_T)
2. Diffusion capacitance (C_D)

The transient capacitance C_T referred to as space charge capacitance or barrier capacitance or depletion region capacitance. C_T is not constant, depends on the magnitude of reverse voltage. The value of C_T is inversely proportional to the width of depletion region and the width of depletion region is directly proportional the reverse voltage.

When the p-n junction diode is forward biased, a capacitance which is much larger then the transient capacitance is known as diffusion capacitance (C_D) or storage capacitance.

The diffusion capacitance (C_D) is given by,

$$C_D = \frac{dQ}{dV}$$

Forward A.C. and D.C. resistance of junction

The two types of resistance associated with a p-n junction diode are

1. DC resistance
2. AC resistance

The resitance offered by the diode to the DC operating conditions is called as "DC resistance or Static resistance " denoted by R_F .The DC resitance of a diode at operating point can be obtained by tacking the ratio of V_F & C_D

The resistance offered by the diode to the AC operating conditions is called as "AC resistance or Dynamic resistance" denoted by r_F. AC resistance is actually the reciprocal of the slope of the forward characteristics .

$$r_F = \frac{1}{Slope\ of\ the\ characteristics}$$

Reverse Breakdown

The maximum reverse bais voltage that can be applied to a p-n diode is known as reverse breakdown voltage. The breakdown in a reverse biased diode can take place due to following effects :

1. Avalenche effect
2. Zener effect

Once the breakdown voltage is reached, a large number of the minority carrier suddenly appears in a depletion layer and the diode conducts heavily.

Due to large reverse voltage the velocity of the minority carrier will increase & hence kinetic energy associated with them will also increase. While travelling, these high kinetic energy carriers will collide with the stationary atoms and impart some kinetic energy to the valence electrons present in the covalent bonds. Due to additionally acquired energy, these valence electrons collide with further atoms bounded with covalent bonds, generating more free electrons.

The process continues in the geometric fashion, until the reverse current becomes huge. The breakdown voltage of a diode depends on how heavily doped the diode is. Normal diodes has breakdown usually greater than 50V.

The Zener breakdown occurs in high doping diodes, where as avalanche breakdown occurs at low doping diodes. The breakdown voltage in Zener is lesser then Avelanche breakdown voltage.

Doping ↑ Breakdown voltage ↓

Doping ↓ Breakdown voltage ↑

The maximum reverse voltage that can be applied before entering the breakdown is called Peak inverse voltage (PIV) or Peak reverse voltage (PRV).

Derivations

1. $\frac{\Delta V}{\Delta T}$= -2.5mV/^{0}C
2. ΔV= (-2.5mV/^{0}C) * ΔT
3. % I_S= 100% for a 10^0C increase
4. % I_S= 7% per ^{0}C

Long & Short Questions

Q.1. Explain what is meant by mobility of charge carrier in a solid. Derive an expression for the conductivity of semiconductor containing both electrons & holes in terms concentration and mobilities of charge carriers. [Kanpur 2010]

Related Short Answer Questions

(i) Define mobility of charge carriers in a semiconductor [Kanpur 1993,2000]
(ii) What do you mean by diffusion & diffusion current ? [Kanpur 1995]

Mobility : This is a property of conductor defined as the ratio of drift velocity to applied electric field in a conductor denoted by μ. Let us assume that when unit electric field is applied across the piece of metal causing drift velocity of v meter /sec, since drift velocity is directly proportional to electric field , we have

$$v \propto E \implies v = \mu E$$

$$\therefore \quad \mu = \frac{v}{E}$$

$\therefore$ unit of μ would be $\frac{metere^2}{volt-sec}$

Conductivity : It is measure of the ease at which an current flows through the conductor. It is also defined as the inverse of resistivity denoted by σ:

$$\sigma = \frac{1}{\rho} \qquad (\rho = \text{resistivity})$$

$\therefore$ unit of σ is Siemens / meter

Also $J = \sigma E \implies \sigma = \frac{J}{E} = \frac{ne\mu}{E}$ (J= current density, n=no. of free electrons, e=electronic charge, E= electric field)

$$\therefore \ \sigma = \frac{J}{E} = \frac{1}{\rho}$$

In semiconductors, there are two types of charge carriers (electrons & holes) , therefore the conductivity of semiconductor due to conductivity of electrons(σ_e) & conductivity of holes(σ_h).

$$\sigma_e = \frac{J_e}{E} = \frac{nev_e}{E} = ne\mu_e$$

$$\sigma_h = \frac{J_h}{E} = \frac{pev_h}{E} = pe\mu_h$$

Total conductivity of a semiconductor

$\sigma = \sigma_e + \sigma_h = ne\mu_e + pe\mu_h$ (for intrinsic semiconductor $n = p = n_i$)

$\sigma_i = en_i(\mu_e + \mu_h)$.

Q.2. What are majority and minority charge carriers in n-type & p- type semiconductor ? Explain with diagram . What is doping ? [Kanpur 2005,12]

Minority & Majority Carriers

- In n-type semiconductor there is excessive free electrons so the majority carriers are electrons & holes are minority carriers where as in p-type semiconductor there is excess of holes therefore majority carriers are holes & electrons are minority carriers.
- For intrinsic semiconductor no. of electrons is same as the no. of holes , therefore , there is no minority & majority carriers

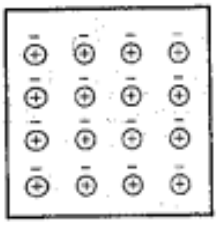


Fig.1 n-type semiconductors

Doping

- Doping is the process of control addition of impurity in pure semi conductor , due to which conducting properties of semiconductor changes. The doped semiconductor is known as Extrinsic semiconductor .
- The impurities may be of two types

  1. Donor impurity 2. Acceptor impurity
- Donor impurity(pentavalent atom) is used to manufacture n-type extrinsic-semiconductor.
- Acceptor impurity (trivalent atom) is used to manufacture p-type extrinsic- semiconductor.
- We visualized the pentavalent atoms and free electrons n- type semiconductors as shown in fig.1 . Each circled plus sign represents a pentavalent atom, and each minus sign is the free electron
- Similarly we visualized the trivalent atoms and free holes p- type semiconductors as shown in fig. Each circled plus sign represents a trivalent atom, and each plus sign is the hole.

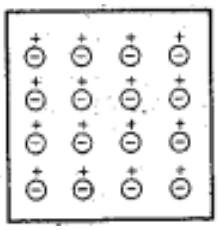


Fig. 2 p-type semiconductors

Q.3. **Derive expression for the densities of free electrons and holes in an instrinsic semiconductor. Show that the Fermi level lies half way between the conduction and valence bands. [Kanpur 92,94,97,98,2011,2013 important]**

Related Short Answer Questions

(i) Define and explain 'Fermi Level' [Kanpur 2010]

(ii) Define law of mass action

- In an intrinsic semiconductor , concentration of free electrons and holes is equal. Theoretical analysis reveals that under thermal equilibrium the product of concentration of free electrons and holes is constant. This is known as **law of mass action.**

$$np = n_i^2$$

Where n_i is the intrinsic concentration and is the function of temperature. For an intrinsic semiconductor $n = p = n_i$

Fermi level

- Fermi level is simply a reference energy level. It is the energy level at which probability of finding electron n energy units above it in the conduction band is equal to probability of finding a hole n energy units below it in valence band.
- Let at any temp. T^0 K , no. of electrons in the conduction band be n_C, no. of electrons in the valence band be n_V and total no. of electrons in both band, $n = n_C + n_V$
- No. of electrons in conduction band, $n_C = nP(E_G)$
  Where $P(E_G)$ represents the probability of an electron having energy E_G. Its value may be determined from Fermi-Dirac probability distribution function given as

$$P(E) = \frac{1}{1 + e^{\frac{E_G - E_F}{KT}}}$$

$P(E)$ is the probability of finding an electron having any particular value of energy E.

- The probability $P(0)$ of an electron being found in the valence band with zero energy is

$$P(0) = \frac{1}{1 + e^{\frac{0 - E_F}{KT}}} = \frac{1}{1 + e^{\frac{-E_F}{KT}}}$$

So $$n_V = \frac{1}{1 + e^{\frac{-E_F}{KT}}}$$

Similarly $$n_C = \frac{n}{1 + e^{\frac{E_G - E_F}{KT}}}$$

Now, total no. of electrons in both the bands,

$$n = n_C + n_V = \frac{n}{1 + e^{\frac{E_G - E_F}{KT}}} + \frac{1}{1 + e^{\frac{-E_F}{KT}}} \quad \{\text{if n=1}\}$$

$$\Rightarrow \qquad 1 - \frac{1}{1 + e^{\frac{-E_F}{KT}}} = \frac{1}{1 + e^{\frac{E_G - E_F}{KT}}}$$

$$\Rightarrow \qquad E_F = \frac{1}{2} E_G$$

Q. 4. Describe diffusion of carriers in semiconductor.

- The movement of charge carriers from the region of high carrier concentration to the areas of low concentration, recombination of charge carriers occurs, the process is known as diffusion of carriers.
- The rate at which diffusion occurs depends on the velocity at which carriers move and on the distance between the carriers.
- This diffusion current is proportional to the concentration gradient :

$$J_{nd} = q.D_n.\frac{\partial n}{\partial x}$$
$$J_{pd} = -\, q.D_p.\frac{\partial p}{\partial x}$$

Where D_n and D_p are the diffusion constant of p and n- type semiconductor.

- Generally free electrons moves in conduction band & holes in valence band , valence band is more effected by electrostatic force so , we say mobility(it is the ease with which charge carriers flow) of electrons is higher then that of holes .

- The mobility of electron being higher than that of holes, the Einstein relationship shows that, for a given concentration gradient, the diffusion current for electrons is higher than the diffusion current for holes.

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{q}$$

Q.5 What is p-n junction diode? How does a barrier field appear across a p-n junction ?

[Agra 2008,11]

Or

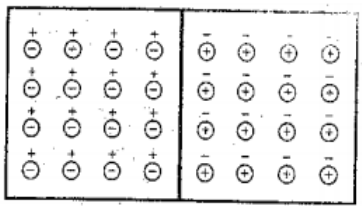
Explain the pn junction at no bias

Related Short Answer Questions

(i) Explain the term diode .

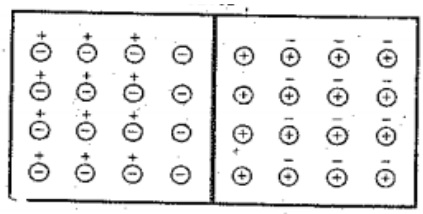
Junction Diode

- The border b/w p-type and n-type semiconductor is called p-n junction, which has led to different inventions including diodes, transistors and integrated circuits.



- We visualized the pentavalent atoms and free electrons n- type semiconductors as shown on the right side of fig. . Each circled plus sign represents a pentavalent atom, and each minus sign is the free electron it contributes to the semiconductor .

Two types of semiconductors



- A manufacturer can produce a single crystal with p-type material on one side and n-type on the other side ,the region where these materials meet known as junction diode.

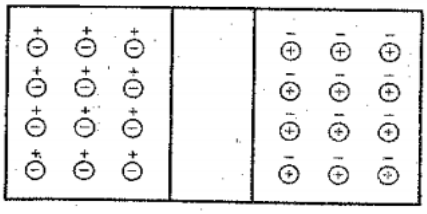
Barrier Potential

- The free electrons on n side tend to diffuse across the junction , when free electrons enters the p region, it recombines with hole, and due to which hole disappears and free electron becomes valence electron.

Creation of ions at junction

- Each time an electron diffuses across a junction , it creates a pair of ions , +ve ion on n side and -ve ion on p side, these pair of ions at junction is called a dipole. As no. of dipoles builds up, empty charge region is created know as depletion region.
- Each dipole has electric field b/w the +ve & -ve ions. Therefore , if additional free electrons enters the depletion region, the electric field tries to push these electrons back into the n region. The electric field b/w the ions is equivalent to difference of potential called the barrier potential.

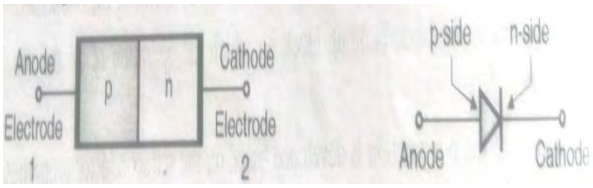
Depletion layer



The pn junction

Diode

- The pn- junction itself forms the most basic semiconductor device called semiconductor diode. Thus semiconductor diode and pn junction are one and the same.
- The meaning of the term "diode" is the device having "two electrodes" (di-ode).
- As shown in fig., the diode has two electrodes one each for the two regions on each side of the junction.
- The two electrodes named as anode and cathode



The current will flow through the diode, if and only if an external voltage source is connected to it with appropriate polarities.

Q.6 Explain with suitable diagrams, why the energy levels of an atom becomes energy band in solids and hence explain the behavior of conductors, semiconductors and insulators.

or [Kanpur 1992]

What do you mean by energy band ? Distinguish clearly between a metal, semiconductors and insulator on the basis of energy bands in solids. [Kanpur 1994,97]

or

Why the energy levels of an atom become energy band in solids and hence explain the distinction between solid conductors, semiconductors and insulators. [Kanpur 1995, 2002]

Or

What do you mean by energy band in solids ? How are they formed ? How can you make a distinction between metal, insulators and semiconductor on the basis of these bands.

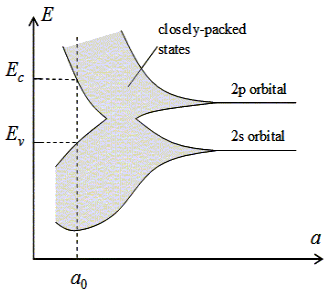
[Kanpur 1999]

Related Short Answer Questions

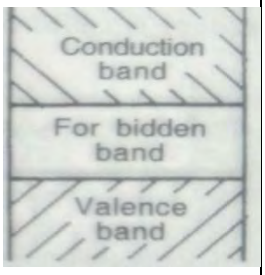
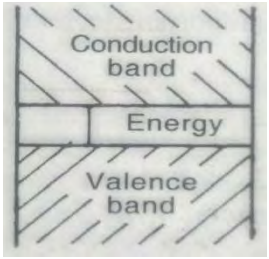
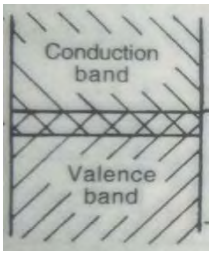
(i) Distinguish metals, insulators and semiconductors [Kanpur 2004]

(ii) Explain conduction and valance band [Kanpur 2009]

- In an isolated atom electrons are restricted to sets of discrete energy levels, with large gaps among them where no energy state is available for the electron to occupy.
- When these isolated atoms are brought together (interatomic spacing) to form a solid, various interactions (attraction and repulsion) occur between atoms, due to which same energy level has distinct value in different atom i.e. a same energy level has a band of energy.
- As interatomic spacing is decreased as shown in the fig., the energy band formed ,splits into two band separated by energy gap, known as forbidden gap.
- The higher energy band (upper band) is known as conduction band and the lower ener called valence band.



Conductor , Semiconductor & Insulators

Characteristics	**Insulator**	**Semiconductor**	**Conductor**
Conductivity	Low	Moderate	Vary High
Resistivity	Vary High	Moderate	Vary Low
Electrons availability	small	moderate	large
Energy band diagram			
Temperature coefficient	Negative	Negative	Positive
Forbidden gap	Large	Small	No gap
Examples	Paper, Mica, glass	Silicon, Germinium	Matels, Aluminium, Copper

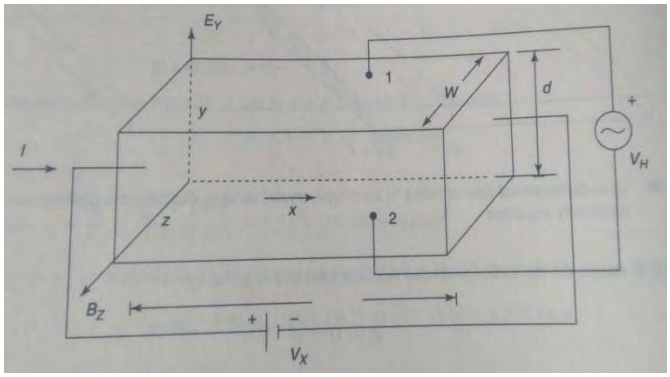
Q.7. What is hall effect ? Obtain expression for hall coefficient and hall voltage and describe method for its determination. [Kanpur 2009]

Related Short Answer Questions

(i) Define Hall co-efficient.

(ii) Why is Hall Potential developed ?

When a semiconductor sample carrying a current I is placed in a transverse magnetic field B, then an electric field E_0 is induced in the specimen , in the direction perpendicular to both B and I , this phenomenon is called the **HALL effect.**



- Hall effect may be used for determining whether a semiconductor is *n*-type or *p*-type .If a current I is applied in the +ve x-direction and magnetic field in +ve z-direction, a force will be exerted in the –ve y-direction of the current carriers.
- The current is carried by electron from side 1 to side 2, if the semiconductor is *n*-type. Therefore Hall voltage appers between surfaces 1 & 2 . The electric field developed in *y*-direction E_y is given by :

$$\frac{\mathrm{V_H}}{d} = \mathrm{E_y}$$

Where , d is the distance between surfaces 1 & 2 . In the equilibrium state the electric field $\mathrm{E_y}$ due to the Hall effect must exert force on the carrier, which just balances the magnetic force i.e.

$$\mathrm{eE_y = Bev_0}$$

where e is magnitude of charge of carriers , $\mathrm{v_0}$ is the drift velocity.
Current density J is given by :

$$J = \rho \mathrm{v_0} = \frac{\mathrm{I}}{wd}$$

Where , ρ is the charge density & w is the width of the specimen in the direction of the magnetic field. Combing all the above relations, we have

$$V_H = E_y d = B v_0 \; d = BJd/\rho = BI/\rho W$$

If the polarity of V_H is +ve at terminal 1 then the carrier must be an electron and $\rho = n_0 e$ where $\mathrm{n_0}$ is the electron concentration . If the terminal 2 becomes positively charged w.r.t. terminal 1 the semiconductor must be of p-type and $\rho = P_0 e$, where P_0 is the hole concentration:

$$R_H = \frac{l}{\rho}$$

Where R_H is the Hall coefficient.

$$R_H = \frac{\mathrm{V_H\ w}}{BI}$$

Conductivity σ is related to p mobility μ by : $\sigma = n_0 e \mu$

$$\sigma = \rho_0 \mu \qquad \Rightarrow \frac{1}{\rho_0} = \frac{\mu}{\sigma}$$

where, $\rho = n_0 e$

If the conductivity is measured with Hall coefficient, mobility μ can be determined by :

$$\because \quad J = \sigma E = \rho \mu E$$

$$\therefore \quad \frac{1}{\rho} = \frac{\mu}{\sigma} = R_H$$

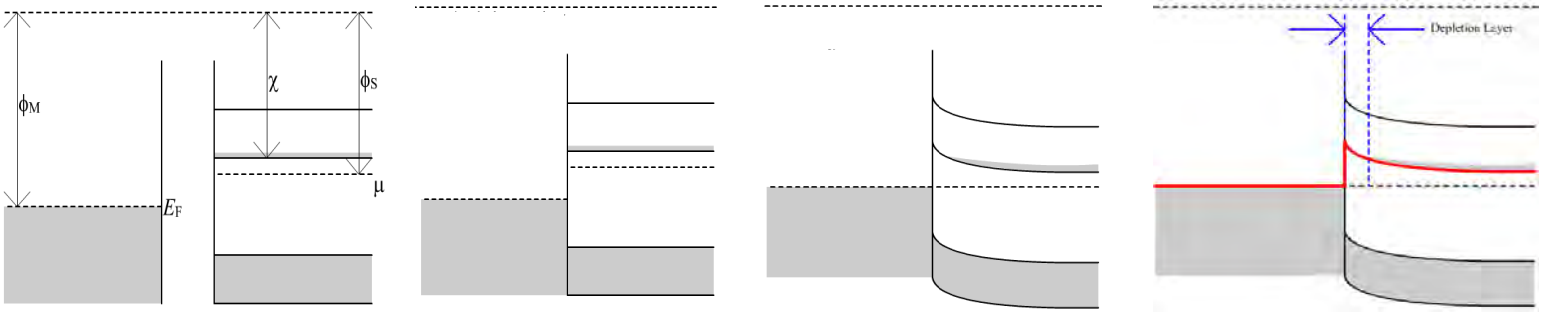
$$\therefore \qquad \mu = \sigma R_H$$

In the presence of scattering the mobility can be approximately be written as :

$$\mu = \frac{8\sigma}{3\pi} R_H$$

Q.8 Explain work function in metals and semiconductor junction.

- Energy required for an electron to move from Fermi level into the free space known as work function .
- The schematic below in fig. a shows a metal and an *n*-type semiconductor. The dashed line at the top represents the zero of energy of free space.
- In fig. a, the work functions of metal & semi conductor denoted by Φ_M & Φ_S resp., E_F & μ indicates the fermi level of metal & semi conductor resp, χ i.e. electron effinity.

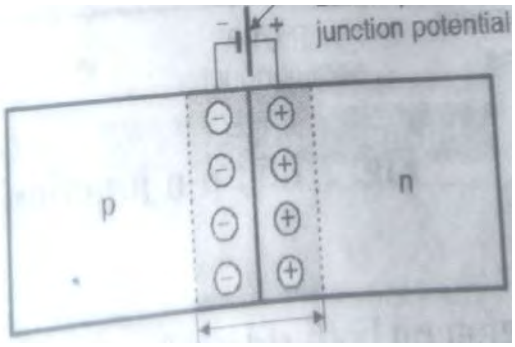


(a) (b) (c) (d)

- When contact is made as shown in fig. b, electrons lower their energy by flowing from the semiconductor conduction band into the metal.
- This continues until the fermi energy level in the semiconductor as shown in fig. c reaches equilibrium with the fermi energy of the metal.
- The deformed band structure shown in fig. d known as depletion layer forms a potential barrier.

Q.9 Explain junction potential width of depletion layer.

- Width of depletion layer is the distance measured from one side to the other side of the depletion region.
- Due to the presence of depletion region the electrons and holes do not i.e. depletion region acts as a barrier.
- Due to the presence of immobile +ve (n-side) and –ve(p-side) ions on opposite sides of the junction an electric field is created across the junction . This electric field is known as junction potential.
- Also known as barrier potential , as it act as a barrier to oppose the flow of electrons and holes across the junction.
- Barrier potential is measured in volts. The barrier



potential for silicon is 0.7 volt whereas for germanium is 0.3 volt at 25^0C.

- The built in potential V_{bi} at diode junction is

$$V_{bi} = \frac{KT}{q} \ln \left(\frac{N_A N_D}{N_i^2}\right)$$

where N_A = Acceptor [ ], N_D = Donor [ ] , N_i = instrinsic [ ] , K= Boltzmann constant

- The width d of depletion region is

$$d = \sqrt{\frac{2\xi_0}{q}} \left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_{bi}$$

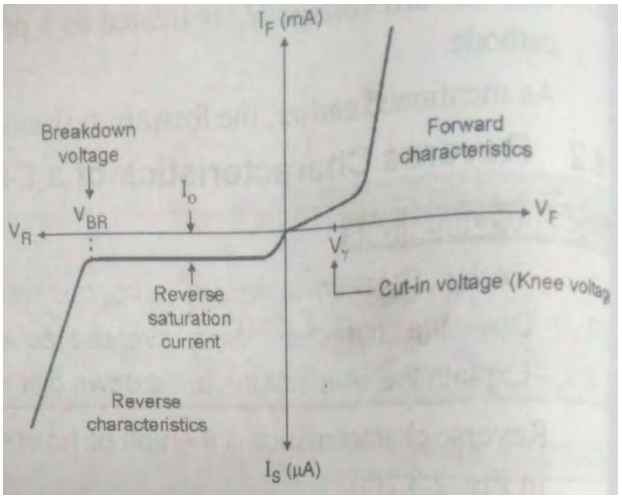
Q.10 Draw & explain the characteristic curve of P-N Junction diode . [Kanpur 2014, important]

Or

Explain the effect of temperature on the reverse saturation current in a junction diode. [Kanpur 2015, important]

The V-I characteristics of p-n junction diode is a graph of voltage across the diode versus the current flowing through it . The V-I characteristics can be dived into two parts i.e. forward & reverse characteristics. The right side & left side of graph is forward & reverse characteristics respectively.

Forward characteristics



- When the external voltage is applied on germanium (Ge)/silicon (Si)diode, is less then 0.3/0.7 volts , the Ge/Si diode allows negligible current to flow through it know as cut in voltage & the Cut off region of V-I characteristics.
- When the external voltage is applied on germanium (Ge)/silicon (Si)diode, is more above cut in voltage, current through the diode increases suddenly.
- The voltage at which the forward diode current increases rapidly is known as cut in voltage or Knee voltage. Knee voltage for Ge is 0.3V & for Si is 0.7V.
- The Forward characteristics of Si diode shifts to the left at a rate of 2.5mV per ^{0}C increase in temperature.

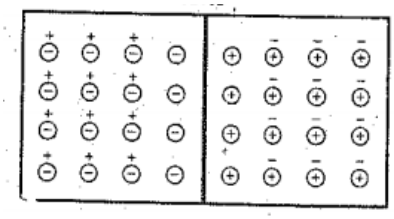
Reverse characteristics

- Current flowing through a diode in the reverse biased state is known as reverse saturation current.

- As the reverse voltage is increased but below breakdown voltage(V_{BR}) , the reverse saturation current remains constant, if the temperature is constant . However when the reverse voltage is above (V_{BR}) , the large current flows
- The reverse saturation current in Si increases 100 % for each 10^0C rise in temperature i.e. approximately equal to 7 % for each ^{0}C rise in temperature.

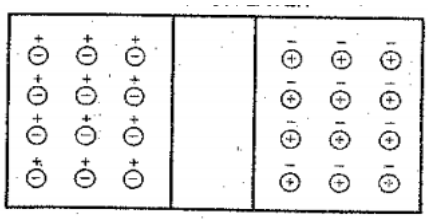
Q.11 Discuss the meaning of potential barrier &Junction capacitance of a P-N junction diode
or [Kanpur 2015]

Explain field and capacitance of depletion layer.



Creation of ions at junction

Depletion layer



The pn junction

Barrier Potential

- The free electrons on n side tend to diffuse across the junction , when free electrons enters the p region, it recombines with hole, and due to which hole disappears and free electron becomes valence electron.
- Each time an electron diffuses across a junction , it creates a pair of ions , +ve ion on n side and -ve ion on p side, these pair of ions at junction is called a dipole. As no. of dipoles builds up, empty charge region is created know as depletion region.
- Each dipole has electric field b/w the +ve & -ve ions. Therefore , if additional free electrons enters the depletion region, the electric field tries to push these electrons back into the n region. The electric field b/w the ions is equivalent to difference of potential called the barrier potential.

The two types of capacitances associated with a p-n junction diode are

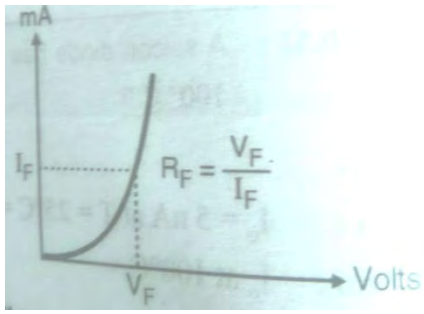
1. Transition capacitance (C_T)
2. Diffusion capacitance (C_D)

- The **transient capacitance** C_T referred to as space charge capacitance or barrier capacitance or depletion region capacitance.
- C_T is not constant, depends on the magnitude of reverse voltage.
- The value of C_T is inversely proportional to the width of depletion region and the width of depletion region is directly proportional the reverse voltage.
- When the p-n junction diode is forward biased, a capacitance which is much larger then the transient capacitance is known as **diffusion capacitance** (C_D) or storage capacitance.
- The diffusion capacitance (C_D) is given by ,

$$C_D = \frac{dQ}{dV} = \frac{dI(V)}{dV} T_F \text{ , where } T_F = transist\ time$$

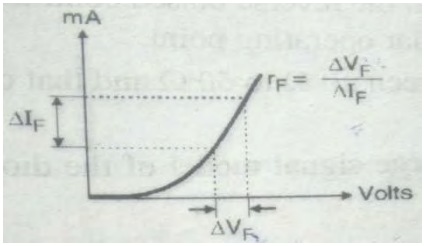
Q.12 Explain how you will determine the static & dynamic resistance of p-n junction.
Or
Differentiate between static & dynamic resistance of a diode.
Or
Discuss A.C. and D.C. resistance of junction

two types of resistance associated with a p-n junction diode are



1. DC resistance
2. AC resistance

- The resitance offered by the diode to the DC operating conditions is called as "DC resistance or Static resistance " denoted by R_F
- The DC resitance of a diode at operating point can be obtained by tacking the ratio of V_F & C_D



- The resistance offered by the diode to the AC operating conditions is called as "AC resistance or Dynamic resistance" denoted by r_F.
- AC resistance is actually the reciprocal of the slope of the forward characteristics .

$$r_F = \frac{1}{Slope\ of\ the\ characteristics}$$

Q.13. Discuss the different types of junction breakdown that can occur in a reverse biased diode.

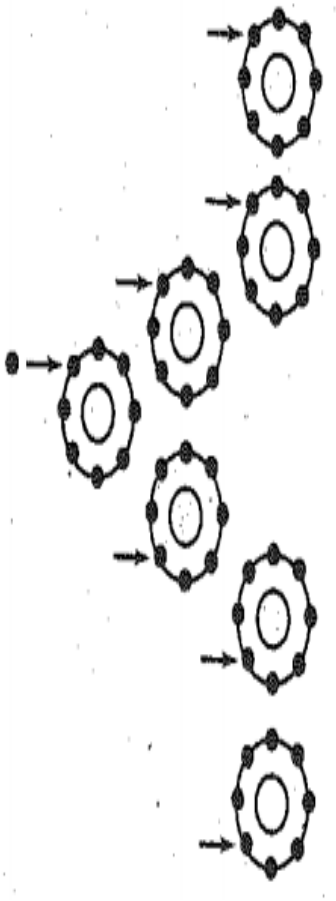
Or

What do you mean by Zener & Avalanche breakdown in the barrier layer of a semiconductor ?

Or

Explain the two breakdown mechanisms of a reverse bias diode.

- The maximum reverse bais voltage that can be applied to a p-n diode is known as **reverse breakdown voltage**.
- The breakdown in a reverse biased diode can take place due to following effects :
  1. Avalenche effect
  2. Zener effect



- Once the breakdown voltage is reached , a large number of the minority carrier suddenly appears in a depletion layer and the diode conducts heavily.
- Due to large reverse voltage the velocity of the minority carrier will increase & hence kinetic energy associated with them will also increase.
- While travelling, these high kinetic energy carriers will collide with the stationary atoms and impart some kinetic energy to the valence electrons present in the covalent bonds.
- Due to additionally acquired energy, these valence electrons collide with further atoms bounded with covalent bonds, generating more free electrons.
- The process continues in the geometric fashion , until the reverse current becomes huge.
- The breakdown voltage of a diode depends on how heavily doped the diode is. Normal diodes has breakdown usually greater than 50V.
- The Zener breakdown occurs in high doping diodes, where as avalanche breakdown occurs at low doping diodes.
- The Zener breakdown voltage is lesser then Avelanche breakdown voltage.
- Doping ↑ Breakdown voltage ↓

Doping ↓ Breakdown voltage ↑

- If the breakdown occurs at -4v it is zener breakdown, but if the breakdown occurs above -6v it is avalanche breakdown , however if breakdown occurs between -4v to -6v , it may be avelance or zener breakdown.

Q.14 Define mobility of charge carriers in a semiconductor. Derive expressions for their drift conduction and diffusion conduction. [Kanpur 1993,2000]

Or

What do you mean by diffusion & diffusion current ? Find an expression for the total electron current and hole current in a semiconductor. [Kanpur 1995]

Mobility : This is a property of conductor defined as the ratio of drift velocity to applied electric field in a conductor denoted by μ. Let us assume that when unit electric field is applied across the piece of metal causing drift velocity of v meter /sec, since drift velocity is directly proportional to electric field , we have

$$v \propto E \implies v = \mu E$$

$$\therefore \quad \mu = \frac{v}{E}$$

$\therefore$ unit of μ would be $\frac{metere^2}{volt-sec}$

The Current flowing through the semiconductor due to diffusion of carriers is known as **diffusion Conduction**, the diffusion current density is directily proportional to concentration gradient

$$J_n \propto \frac{dn}{dx} \implies J_n = qD_n \frac{dn}{dx}$$

$$J_p \propto \frac{dp}{dx} \implies J_n = -qD_p \frac{dp}{dx}$$

Where D_n & D_p are diffusion constants for n-type & p-type semiconductors

Einstein rel^n

$$D_n \propto \mu_n$$

$$D_p \propto \mu_p$$

$$\frac{D_n}{D_p} = \frac{\mu_n}{\mu_p} = V_T = \frac{KT}{q}$$

Current flowing through the semiconductor under the applied E-field called **Drift current**

$$J_n = qn\mu_n E$$

$$J_p = qn\mu_p E$$

Numerical

Q.1 Find the conductivity (σ) & resistivity (ρ) of an instrinsic semiconductor at temp. of 300^0K. It is given that n_i=2.5 x 10^{13}/cm^3, μ_n=3,800cm^2/sV, μ_p=1,800cm^2/sV , q= 1.6 x10^{-19} C.

Exp: As n_i=2.5 x 10^{13}/cm^3

μ_n=3,800cm^2/sV,

μ_p=1,800cm^2/sV ,

q= 1.6 x10^{-19} C

∵ Conductivity of instrinsic semiconductor (σ_i)= n_i e(μ_n + μ_p)

∴ σ_i = 2.5 x 10^{13} x1.6 x10^{-19} (3,800+ 1800) = 0.0224 S/cm Ans

∵ ρ_i= 1/ σ_i = 1/0.0224 = 44.64 Ω-cm Ans

Q.2. The instrinsic carrier concentration for silicon at room temperature (300^0K) is 1.5x 10^{10}/cm^3. If the mobility of electrons and holes are 1300cm^2/sV & 450cm^2/sV resp. what is the conductivity of silion at 300^0K ? If silicon is doped with 10^{18} boron atoms /cm^3, what is its conductivity ?

Exp: Given n_i=1.5x10^{10}/cm^3

μ_n=1300cm^2/sV,

μ_p=450cm^2/sV

∵ Conductivity of instrinsic semiconductor (σ_i)= n_i e(μ_n + μ_p)

∴ σ_i = 1.5x10^{10} x1.6 x10^{-19} (1300+ 450)=4.2 x 10^{-6}

∵ N_A= 10^{18} / cm^3

∴ Conductivity of a resulting P-type silicon semiconductor, σ_p =e N_A μ_p= 1.6 x10^{-19} x10^{18} x450

= 72S/cm Ans

Q.3. If germanium is doped with 2x 10^{21}atoms /m^3 atoms of aluminium then determine (i) Hole concentration (ii) concentration of free electrons (iii) conductivity at room temperature. Given μ_n=0.17 m/sec/v/m, E_g=0.7eV. [Kanpur 1996,2003]

Exp: If we assume that all the acceptor atoms contributes to conduction then

Hole concentration = 2x 10^{21}atoms /m^3

The free electron density in intrinsic semiconductor

$n_i = N_C e^{-(E_c - E_f)/KT}$, where $N_C = 2(2\pi m_e kT/h^2)^{3/2}$

$= 2*\left(\frac{2*3.14*9.1x10^{-31}*1.38x10^{-23}*300}{6.6*10^{-34}}\right)^{\frac{3}{2}} e^{\frac{-0.7*1.6*10^{-19}}{2*1.38*10^{-23}}}$

$= 2.4x\ 10^{19}$ electron /cm^3

∴ The no. of free electrons $n = (n_i)^2/p = (2.4x\ 10^{19})^2/2x\ 10^{21} = 2.8 \times 10^{17}$

Conductivity $\sigma = ep\ \mu_n = 1.6\ x10^{-19} x\ 2x10^{21} x0.17 = 54.4$mhv.

Q.4. In an N-type semiconductor, the Fermi level lies 0.5 eV below the conduction band. If the concentration of doner atoms is tripled, find the new position of the fermi level, taking the value kT=0.3eV. [Kanpur 2013]

Exp: $E_C - E_F = 0.5$eV at a given conc^n (let it be N_D)

New conc^n $(N'_d) = 3* N_D$

Let new fermi levl position be E'_f

We know that $n=n_d=N_e e^{\frac{E_f - E_c}{kT}}$

$$\frac{N'_d}{N_d} = \frac{e^{\frac{E'_f - E_c}{kT}}}{e^{\frac{E_f - E_c}{kT}}}$$

$$\Longrightarrow 3 = \frac{e^{\frac{0.5}{kT}}}{e^{\frac{E_f - E_c}{kT}}} \quad \text{(taking } ln \text{ both sides)}$$

$$\Longrightarrow \ln 3 = \frac{0.5 + (E_f - E_c)}{0.03} \quad (kT = 0.03eV)$$

$$\Longrightarrow E_C = E_C - 0.5eV.\ \ln 3 \text{ Ans}$$

Q.5 A sample of intrinsic germanium at room temperature has a carrier concentration of 2.4 * $10^{19}/m^3$. It is doped with anitimony at a rate of one antimony atom / 10^8 atom of germanium atom. If the concentration of germanium atom is $4*10^{28}$ atoms/m^3, find the hole concentration and conductivity of the semiconductor. Mobility of electron $\mu_n = 0.35 m^2$/V-sec. [Kanpur 2006]

Exp: Given $n_i = 2.4 * 10^{19}$, $N = 4*10^{28}$

$N_D/N = 1: 10^8$

∴ $N_D = 4*10^{28}/10^8 = 4*10^{22}$ doners/m^3

$n \sim N_D = 4*10^{22}$ electrons / m^3

∴ $p = n_i^2/N_D = (4*10^{28})^2/4*10^{22} = 1.4 *10^{16}$holes /$m^3$

Q.6. Calculate the conductivity & resistivity of a p-type Ge crystal which is mixed by acceptor atoms of concentration $2*10^{17}$atoms/ cm^3 & all acceptor atoms are active , given that μ_h=1900cm^2/volts-sec, e=$1.6*10^{-19}$coulomb [Kanpur 1999]

Exp: Given $n_h = 2*10^{17}$atoms/ cm^3= $2*10^{23}$ atoms/m^3 ,

μ_h=1900cm^2/volts= 0.19 m^2/volts

$\because \sigma_p = e\, n_h * \mu_h$

$\therefore \sigma_p = 1.6*10^{-19}*2*10^{23}*0.19 = 6080$ mho /m

$\because \rho_p = 1/\sigma_p$

$\therefore \rho_p = 1/6080\ \Omega$-m

Q.7. A silicon bar is doped with donor impurities $N_D = 2.25 \times 10^{15}$ atoms / cm^3. Given the intrinsic carrier concentration of silicon at T = 300 K is $n_i = 1.5 \times 10^{10}$ cm^{-3}. Assuming complete impurity ionization, find the equilibrium electron and hole concentrations .

Exp: As per the given data

$N_D = 2.25 \times 10^{15}$ Atom / cm^3

$n_i = 1.5 \times 10^{10}$ / cm^3

Since complete ionization taken place,

$n_0 = N_D = 2.25 \times 10^{15}$ / cm^3

$\because P_0 \,.\, n_{0=} n_i^2$

$\therefore P_0 = n_i^2/ n_0 = (1.5 \times 10^{10})^2/2.25 \times 10^{15} = 1*10^5/cm^3$ Ans

Q.8 Assume electronic charge $q = 1.6\times10^{-19}$ C, kT/q = 25 mV and electron mobility $\mu_n = 1000$ cm^2/V-s. If the concentration gradient of electrons injected into a P-type silicon sample is $1\times10^{21}/cm^4$, find the magnitude of electron diffusion current density (in A/cm^2) .

Exp: Given $q = 1.6\times10^{-19}$ C, kT/q = 25 mV, μ_n = 1000 cm^2/V-s.

From Einstin relation ,

$$\frac{D_n}{D_p} = \frac{\mu_n}{\mu_p} = V_T = \frac{KT}{q}$$

$$\Rightarrow D_n = 25mV * 1000cm^2/v - s = 25cm^2/s$$

Diffusion current Density $J = q\, D_n \frac{dn}{dx}$

$= 1.6 \times 10^{-19} \times 25 \times 1\times10^{21}$

$= 4000$ A / cm^2 Ans

Q.9 When a silicon diode having a doping concentration of $N_A = 9 \times 10^{16}$ cm^{-3} on p-side and $N_D = 1 \times 10^{16}$ cm^{-3} on n-side is reverse biased, the total depletion width is found to be 3 µm. Given that the permittivity of silicon is 1.04×10^{-12} F/cm, find the depletion width on the p-side and the maximum electric field in the depletion region.

Exp: Given $N_A = 9 \times 10^{16}$ / cm^3 ; $N_D = 1\times10^{16}$ / cm^3

Total depletion width, $x = x_n + x_p = 3$ µm.

$\in = 1.04 \times 10^{-12}$ F / cm

Since $\frac{X_n}{X_p} = \frac{N_A}{N_D} = = (9 \times 10^{16})/(1 \times 10^{16})$

$X_n = 9X_p$

$\because$ x= x_n+x_p=3 μm.

9 x_p +x_p =3 μm.

$\therefore$ x_p = 0.3 μm

Max. Electric field, E= $qN_AN_D / \in = (1.6*10^{-19} *9 \times 10^{16} * 1\times10^{16}) / (1.04 \times 10^{-12})$

$= 4.15 \times 10^5$ V / cm Ans

Q.10 A diode has a power rating of 5W. if the diode voltage is 1.2 V and the diode current is 17.5 A, what is the power dissipation ? will the diode be destroyed ?

Exp: $\because P_D = V_D I_D$

$\therefore P_D$= (1.2V)(1.75A)=2.1W

$\because P_D$ < 5W so the diode will not destroyed.

Q.11. Find the dynamic resistance of a P-N junction diode at a forward current of 2mA. Assume kT/q= 25mV.

Exp: Given , forward current = 2mA= 0.002A

Volt equivalent of temp. , V_T= **kT/q= 25mV**

$\because$ Dyamic resistance (r) = $\eta V_T/I$ (η=1)

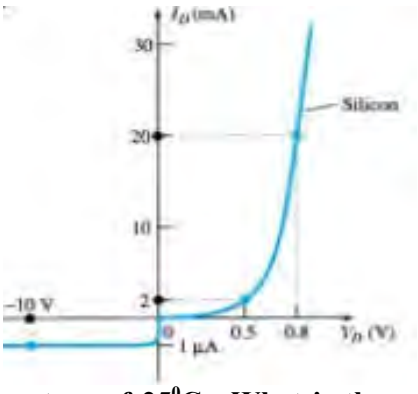
$\therefore$ r = 0.025/0.002= 12.5 Ω.

Q.12 Determine the dc reistance levels for the diode shown in fig. at

(a) $I_D = 2mA$

(b) $I_D = 20mA$

(c) $V_D = -10V$



Exp: (a) At $I_D = 2mA$, $V_D = 0.5\ v$(from the curve)

$\therefore R_D = V_D/I_D$ =0.5v/2mA= 250 Ω

(b) At $I_D = 20mA$, $V_D = 0.8\ v$(from the curve)

$\therefore R_D = V_D/I_D$ =0.8v/20mA = 40 Ω

(c) At $V_D = -10V$, $I_D = -1\mu A$ (from the curve)

$\therefore R_D = V_D/I_D$ =-10v/- 1μA = 10 MΩ

Q.13 Assuming the barrier potential of 0.7V at an ambient temperature of 25^0C , What is the barrier potential of a silicon diode whwn the junction temperature is 100^0C ? At 0^0C ?

Exp: When the Junction temp. is 100^0C , the change in barrier potential is

ΔV= (-2.5mV/^{0}C) ΔT = (-2.5mV/^{0}C)(**100^0C - 25^0C**)= -187.5mV

$\therefore$ The barrier potential will decrese by 187.5mV

i.e. V_B= 0.7V – 0.18V = 0.52 V Ans

When the Junction temp. is 0^0C , the change in barrier potential is

$\Delta V = (-2.5mV/^0C)\ \Delta T = (-2.5mV/^0C)(\ \mathbf{0^0C - 25^0C}) = 62.5mV$

$\therefore$ The barrier potential will increase by 62.5mV

i.e. $V_B = 0.7V = 0.0625 = 0.7625$ V Ans

Q.14. A Silicon diode has a saturaration current of 5nA at 25^0C . What is the saturation current at 100^0C ?

Exp: The change in temp

$\therefore \Delta T = 100^0C - 25^0C = 75\ ^0C$

$\because$ there is seven doubling between 25^0C to 95 ^{0}C

$\therefore \quad I_S = (2^7)(5nA) = 640nA$

$\because$ there is 5 ^{0}C rise in temp from 95^0C to 100 ^{0}C

$\therefore \quad I_S = (1.07^5)(640nA) = 898nA$ Ans

Chapter-2
Semiconductor Devices

pn Junction

It is a border between p-type & n-type semiconductor. The pn- junction itself forms the most basic semiconductor device called semiconductor diode, thus semiconductor diode and pn junction are one and the same.

Depletion layer

In pn junction diode the the free electrons on n side tend to diffuse across the junction ,when free electrons enters the p region, the free electrons recombines with hole in p region, and due to which hole disappears and free electron becomes valence electron.

Each time an electron diffuses across a junction , it creates a pair of ions , +ve ion on n side and -ve ion on p side, these pair of ions at junction is called a dipole. As no. of dipoles builds up, empty charge region is created know as depletion region.

Junction Potential width of depletion layer

Width of depletion layer is the distance measured from one side to the other side of the depletion region. Due to the presence of depletion region the electrons and holes do not i.e. depletion region acts as a barrier. Due to the presence of immobile +ve(n-side) and –ve (p-side) ions on opposite sides of the junction an electric field is created across the junction . This electric field is known as junction potential also known as barrier potential. The barrier potential for silicon is 0.7 volt whereas for germanium is 0.3 volt at 25^0C.

The Energy Hill

The barrier potential of a diode looks like an energy hill. Electrons attempting to cross the junction need to have enough energy to climb this hill. An external voltage source that forward-bias the diode gives electrons the energy required to pass through the depletion layer.

Barrier Potential & Temperature

When the junction temperature increases, the depletion layer becomes narrow & the barrier potential decreases. It will decrease approximately 2.5 mV for each ^{0}C increase.

Forward bias & Reverse bias

When an external voltage opposes the junction potential, the diode is forward biased. If the applied voltage is greater than the barrier potential, the current flows. When an external voltage aids the barrier potential, the diode is reverse biased.

Knee Voltage or Cut-in voltage

The voltage at which the forward diode current increases rapidly is known as Knee voltage or cut in voltage . Knee voltage for germanium is 0.3V & for silicon is 0.7V.

Peak Inverse voltage

The maximum reverse bais voltage that p-n diode can withstand without breaking down is known as peak inverse voltage.

Reverse saturation current

Current flowing through a diode in the reverse biased state is known as reverse saturation current (I_S). The reverse saturation current in Si increases 100 % for each 10^0C rise in temperature i.e. approximately equal to 7 % for each ^{0}C rise in temperature.

Reverse Breakdown

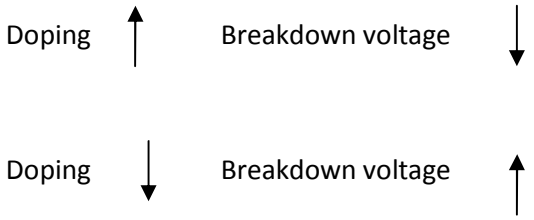
The reverse bais voltage above PIV leads to breakdown of voltage . The breakdown in a reverse biased diode can take place due to following effects :

1. Avalenche Breakdown
2. Zener Breakdown

Once the breakdown voltage is reached, a large number of the minority carrier suddenly appears in a depletion layer and the diode conducts heavily.

Due to large reverse voltage the velocity of the minority carrier will increase & hence kinetic energy associated with them will also increase. While travelling, these high kinetic energy carriers will collide

with the stationary atoms and impart some kinetic energy to the valence electrons present in the covalent bonds. Due to additionally acquired energy, these valence electrons collide with further atoms bounded with covalent bonds, generating more free electrons.
The process continues in the geometric fashion, until the reverse current becomes huge. The breakdown voltage of a diode depends on how heavily doped the diode is. Normal diodes has breakdown usually greater than 50V.
The Zener breakdown occurs in high doping diodes known as **Zener diodes** , where as avalanche breakdown occurs at low doping diodes known as **Avelanche diodes** . The breakdown voltage in Zener is lesser then Avelanche breakdown voltage.



Capacitance of depletion layer
The accumulation of charge across the depletion region produces capacitance action ,where depletion region acts as dielectric medium of the parallel plate capacitor(p-side and n-side as a plates of capacitor)
Transition capacitance (C_T) & Diffusion capacitance (C_D) are two capacitances associated with a p-n junction diode.
Resistance of pn Junction diode
The two types of resistance associated with a p-n junction diode are

1. DC resistance
2. AC resistance

The resitance offered by the diode to the DC operating conditions is called as "DC resistance or Static resistance " denoted by R_F **.**The DC resitance of a diode at operating point can be obtained by tacking the ratio of V_F & C_D
The resistance offered by the diode to the AC operating conditions is called as "AC resistance or Dynamic resistance" denoted by r_F. AC resistance is actually the reciprocal of the slope of the forward characteristics .

$$r_F = \frac{1}{Slope\ of\ the\ characteristics}$$

Tunnel diode
Such a diode having doping level $\approx 10^{25}/m^3$ in both $P-N$ region of pn junction diode known as Tunnel diode. These diodes posses negative resistance & is useful for high-frequency circuits.
Point contact diode
It consists of a small wafer of a semiconducting crystal having an area of few square millimeter & a thickness of a fraction of mm. The crystal is soldered to a metallic base for external ohmic contact.
LED
Light emitting diode (LED) produces electromagnetic energy in the form of light widely used as an indicator on instruments, calculators and other electronic equipment. In ordinary diode energy is radiated in the form of heat but in an LED , the energy is radiated as light.

Photodiodes
Photodiode is a reverse biased P-N junction whose operation depends on the intensity of light .The incoming light produces free electrons and holes. The stronger the light, the greater the number minority carrier and the larger the reverse current.

Thermistors

A thermistor is a device which has negative temperature coefficient useful for making oscillator, amplifiers & switching devices.

Derivations

1. $\frac{\Delta V}{\Delta T}$= -2.5mV/^{0}C
2. ΔV= (-2.5mV/^{0}C) * ΔT
3. % I_S= 100% for a 10^{0}C increase
4. % I_S= 7% per ^{0}C

Long & Short Questions

Q.1. Explain the formation of depletion layer and barrier potential barrier in a p-n Junction diode. Find out the expression for the height of potential barrier and the width of depletion layer. [Important]

Or

Find out the expression for potential barrier and depletion width of a junction diode. [Kanpur 2016]

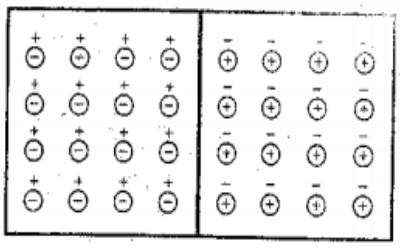
Related Short Answer Question

(i) What is Junction diode? Explain the formation of depletion layer. [Kanpur 2013]

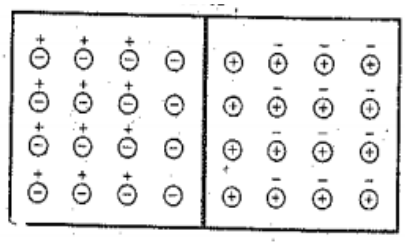
(ii) What is a P-N Junction diode ? How does a barrier field appear across a P-N Junction? [Kanpur 2011]

Formation of depletion layer

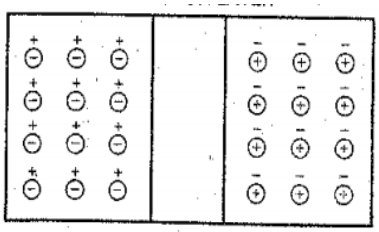
- We visualized the pentavalent atoms and free electrons n- type semiconductors as shown on the right side of fig. . Each circled plus sign represents a pentavalent atom, and each minus sign is the free electron it contributes to the semiconductor .
- A manufacturer can produce a single crystal with p-type material on one side and n-type on the other side ,the region where these materials meet known as junction diode.



Two types of semiconductors



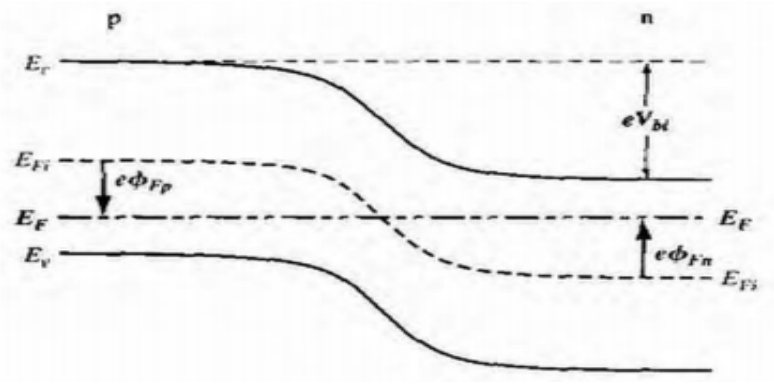
Two types of semiconductors



Creation of ions at junction

- The free electrons on n side tend to diffuse across the junction , when free electrons enters the p region, it recombines with hole, and due to which hole disappears and free electron becomes valence electron.
- Each time an electron diffuses across a junction , it creates a pair of ions , +ve ion on n side and -ve ion on p side, these pair of ions at junction is called a dipole. As no. of dipoles builds up, empty charge region is created know as depletion region.

Expression for barrier potential



Energy Band diagram of a pn junction in thermal equilibrium.

The barrier potential maintains equilibrium , so no current is produced by this voltage. The intrinsic Fermi level is equidistant from the conduction band edge through the junction, thus the built-in potential barrier can be determined as the difference between the intrinsic Fermi level in the p and n regions.

i.e. $V_{bi}= | \Phi_{Fn} | + | \Phi_{Fp} |$ (1)

In the n region, the electron concentration in the conduction band is given by

$$n_0 = n_i \exp^{-(E_C - E_F)/KT} \quad (2)$$

Where n_i& E_{Fi} are the intrinsic carrier concentration and instrinsic fermi energy resp. If Φ_{Fn} is the potential in the n –region $e\,\Phi_{Fn}= E_C - E_F$ (3)

Eq. (3) may be written as

$$n_0= n_i \exp^{-e\,\Phi_{Fn}/KT} \quad (4)$$

Taking natural log both sides, setting $n_0=N_D$

$$\ln(N_D / n_i) = -e\Phi Fn/KT \quad (5)$$

$$\Phi_{Fn}= -\frac{KT}{q} * \ln(N_D / n_i) \quad (6)$$

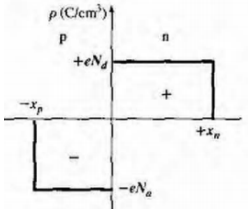
Similarly in p region , the concentration is given by

$$P_0=N_A= n_i \exp^{-(E_F - E_V)/KT} \quad \{\text{since, } e\,\Phi_{Fp}= E_F - E_V\} \quad (7)$$

$$\Phi_{Fp}= \frac{KT}{q} * \ln(N_A / n_i) \quad (8)$$

Substituting eq. (7) & (8) in eq. (1) , we have

$$V_{bi} = \frac{KT}{q} * ln(\frac{N_D N_A}{n_i^2}) = \frac{KT}{q} * ln(\frac{N_D N_A}{n_i^2})$$



Expression for depletion width

Assuming that the space charge region abruptly ends in the n region at $x = x_n$ and abruptly ends in the p region at $x = x_p$, we have

Potential in n region of diode is $\Phi_n(x) = \frac{eN_D}{\epsilon}(x_n\, x - \frac{x^2}{2}) + \frac{eN_A}{2\epsilon_S}x_n^2$ $\quad 0 \leq x \leq x_n$ (9)

Potential in p region of diode is $\Phi_p(x) = \frac{eN_D}{\epsilon}(\frac{x^2}{2} + x_p x) + \frac{eN_A}{2\epsilon_S}x_p^2$ $\quad -x_p \leq x \leq 0$ (10)

The magnitude of potential at $x = x_n$ is equal to built in potential $\mathbf{V_{bi}}$

$$\mathbf{V_{bi}} = \frac{e}{2\epsilon}(N_D x_n^2 \;\; + N_A x_n^2 \;\;) \tag{11}$$

$$\therefore \quad x_n = \{\frac{2\epsilon V_{bi}}{\epsilon}[\frac{N_A}{N_D}][\frac{1}{N_A+N_D}]\}^{\frac{1}{2}} \tag{12}$$

$$\because \quad \frac{X_n}{X_p} = \frac{N_A}{N_D}$$

$$x_p = \{\frac{2\epsilon V_{bi}}{\epsilon}[\frac{N_D}{N_A}][\frac{1}{N_A+N_D}]\}^{\frac{1}{2}} \tag{13}$$

Depletion or space charge width is $W = x_n + x_p$
Using equation (12) & (13) we have

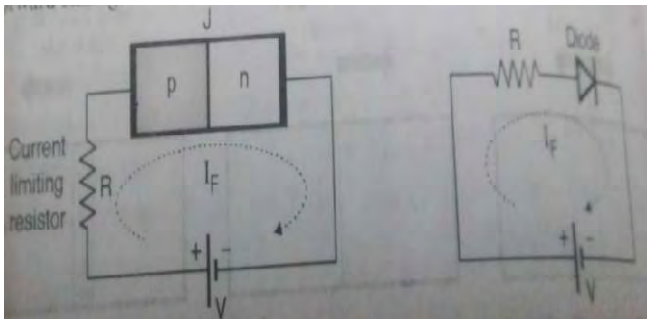
$$W = \{\frac{2\epsilon V_{bi}}{\epsilon}[\frac{N_A+N_D}{N_A N_D}]\}^{\frac{1}{2}} \tag{14}$$

Q.2. Describe the action of forward and reverse biased p-n junction semiconductor. Draw its V-I characteristics curve and explain it. [Kanpur 2014]

Related Short Answer Question

(i) Draw and explain the characteristics curve of a P-N Junction diode. [Kanpur 2014]

Forward bias



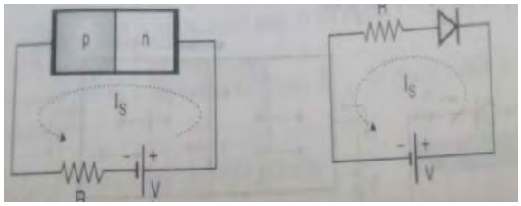
If the p- region(anode) of diode is connected to the +ve terminal of the external DC source and n-region (cathode) is connected to -ve terminal of the external DC source then the biasing is said to "forward biasing".

In forward bias width of depletion layer will reduce

Reverse Bias

If the p- region(anode) of diode is connected to the -ve terminal of the external DC source and n-

region (cathode) is connected to +ve terminal of the external DC source then the biasing is said to "reverse biasing".

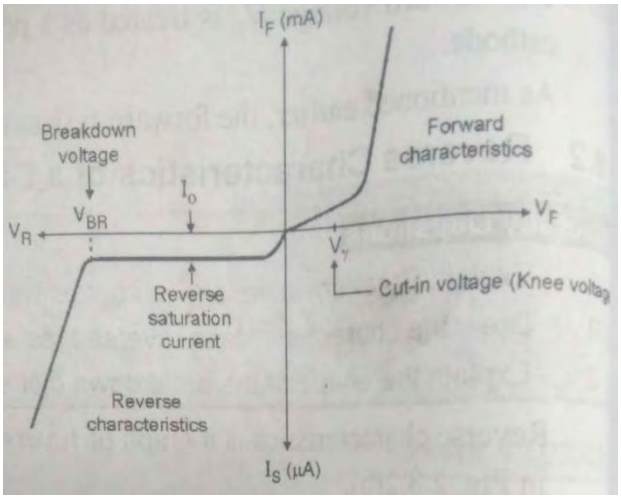


In reverse bias width of depletion layer will increase.

V-I characteristics curve

The V-I characteristics of p-n junction diode is a graph of voltage across the diode versus the current flowing through it . The V-I characteristics can be dived into two parts i.e. forward & reverse characteristics. The right side & left side of graph is forward & reverse characteristics respectively.

Forward characteristics



- When the external voltage is applied on germanium (Ge)/silicon (Si)diode, is less then 0.3/0.7 volts , the Ge/Si diode allows negligible current to flow through it know as cut in voltage & the Cut off region of V-I characteristics.
- When the external voltage is applied on germanium (Ge)/silicon (Si)diode, is more above cut in voltage, current through the diode increases suddenly.
- The voltage at which the forward diode current increases rapidly is known as cut in voltage or Knee voltage. Knee voltage for Ge is 0.3V & for Si is 0.7V.
- The Forward characteristics of Si diode shifts to the left at a rate of 2.5mV per ^{0}C increase in temperature.

Reverse characteristics

- Current flowing through a diode in the reverse biased state is known as reverse saturation current.
- As the reverse voltage is increased but below breakdown voltage(V_{BR}) , the reverse saturation current remains constant, if the temperature is constant . However when the reverse voltage is above (V_{BR}) , the large current flows
- The reverse saturation current in Si increases 100 % for each 10^0C rise in temperature i.e. approximately equal to 7 % for each ^{0}C rise in temperature.

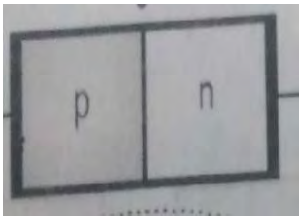
Q.3. What is a junction diode ? What do you mean by biasing a junction diode ? Draw V-I characteristics curve of a junction diode under different biasing . [Important]

Or

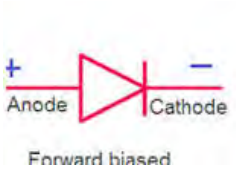
What is junction diode ? Draw its characteristic junction curve. [Kanpur 2016]

Junction Diode

The border b/w p-type and n-type semiconductor is called p-n junction, which has led to different inventions including diodes, transistors and integrated circuits.



Schematic of Junction diode



Symbol of Junction diode

Reaming ref. to Q.2.

Q.4. Discuss the theory of current across p-n junction.

Or

Obtain the current-voltage equation for a p-n junction diode. [Important]

Current across p-n junction

The current in p-n junction flows due to majority & minority carriers present in p & n type semiconductor . The net current density through junction is due to following four contributions

(a) The Current I_1 due to flow of minority electrons from p-type to n-type.
(b) The Current I_2 due to flow of majority electrons from n-type to p-type.
(c) The Current I_3 due to flow of majority holes from p-type to n-type.
(d) The Current I_4 due to flow of minority holes from n-type to p-type.

Therefore $I_{net}= (I_2+I_3) –(I_1+I_4)$

The current density for majority electrons from n-type

$$I_2= A\exp\left[\frac{-e(V_B-V)}{K_B T}\right]$$

Similary for holes $I_3= B\exp\left[\frac{-e(V_B-V)}{K_B T}\right]$

Hear A&B are constant, V_B is barrier and V is the applied voltage.

For no bias condition ,no net current is flowing through the circuit , hence $I_2=I_1$ and $I_3=I_4$

$\therefore \quad I_1 = A\exp\left[\frac{-eV_B}{K_B T}\right]$

$\Longrightarrow \quad A = I_1 / A\exp\left[\frac{-eV_B}{K_B T}\right]$

$\therefore \quad I_2 = I_1 \exp\left[\frac{eV}{K_B T}\right]$

Similarly $I_3 = I_4 \exp\left[\frac{eV}{K_B T}\right]$

$\therefore I_{net} = (I_1 - I_4)\left[\exp\left(\frac{eV}{K_B T}\right) - 1\right] = I_0\left[\exp\left(\frac{eV}{K_B T}\right) - 1\right]$

This equation is known as **Schockley equation**, I_0 is called reverse saturation current.

Q.5. Explain Junction resistance & Junction Capacitance in detail.

Or

Discuss the meaning of potential barrier and junction capacitance of a P-N junction diode

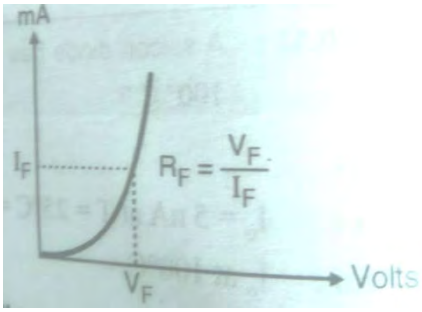
[Kanpur 2015]

Related Short Answer Question

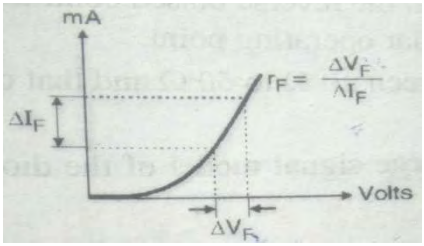
(i) Define resistance of junction diode and obtain expression for them. [Kanpur 2016]

The two types of resistance associated with a p-n junction diode are

1. DC resistance
2. AC resistance



- The resitance offered by the diode to the DC operating conditions is called as "DC resistance or Static resistance " denoted by R_F
- The DC resitance of a diode at operating point can be obtained by tacking the ratio of V_F & C_D



- The resistance offered by the diode to the AC operating conditions is called as "AC resistance or Dynamic resistance" denoted by r_F.
- AC resistance is actually the reciprocal of the slope of the forward characteristics .

$$r_F = \frac{1}{Slope\ of\ the\ characteristics}$$

The two types of capacitances associated with a p-n junction diode are

1. Transition capacitance (C_T)
2. Diffusion capacitance (C_D)

- The **transient capacitance** C_T referred to as space charge capacitance or barrier capacitance or depletion region capacitance.
- C_T is not constant, depends on the magnitude of reverse voltage.
- The value of C_T is inversely proportional to the width of depletion region and the width of depletion region is directly proportional the reverse voltage.
- When the p-n junction diode is forward biased, a capacitance which is much larger then the transient capacitance is known as **diffusion capacitance** (C_D) or storage capacitance.
- The diffusion capacitance (C_D) is given by ,

$$C_D = \frac{dQ}{dV} = \frac{dI(V)}{dV} T_F \text{ , where } T_F = transist\ time$$

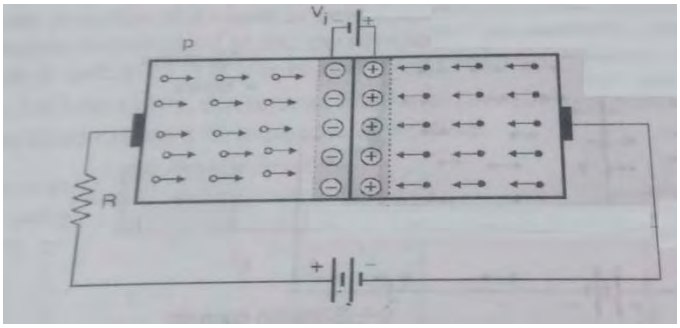
Q.6. How current flow through pn junction ? Discuss effect of biasing on the width of depletion layer

Related Short Answer Question

(i) Draw the energy level diagram with Fermi level for an unbiased, forward biased and reverse biased pn junction. Explain the effect of biasing on the width of depletion layer. [Important]

Mechanism of current flow (Forward bias)

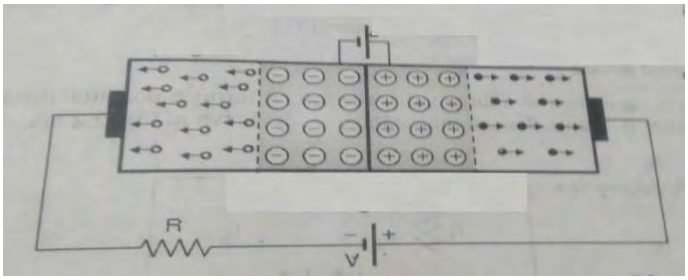
- When diode is forward bias , due to –ve terminal of external source connected to n-region, free electrons from n-side are pushed towards the p-side. Similarly the +ve end of supply will push holes from the p-side towards the n-side.
- With increase in the external supply voltage V, more and more number of holes (p-side) and electrons (n-side) start travelling towards the junction .



- The holes will start converting the negative ions into neutral atoms and the electrons will convert the positive ions into neutral atoms. As a result of this, the width of depletion region will reduce.
- Due to reduction of the depletion region width , the barrier potential will also reduce. Eventually at a particular value of V , the depletion region will collapse. There is absolutely no opposition to the flow of electron and holes.
- The large no. of majority carriers crossing the junction constitute a current called as the forward current.

- The forward current through a p-n junction diode flows due to the majority carriers and its direction of flow(conventional) is always from anode to cathode.
- There is a potential drop across the conducting forward biased diode denoted by V_F equal to 0.7V for silicon & 0.3V for germanium diode.
- The forward voltage drop is due to barrier potential & internal resistance.

Mechanism of current flow (Forward bias)



- When the diode is reverse biased , holes in the p- region are attracted towards the negative terminal of the supply and electrons on the n- side are attracted towards the +ve terminal of the supply.
- **Widening of depletion region** : Due to movement of majority carriers away from the junction , width of depletion layer increases .
- The minority electrons on p-side are attracted by +ve end of dc supply. Hence these electrons will cross the junction and constitute the reverse current I_S of the diode.
- The reverse current flows due to minority carriers is also called as the "Reverse Saturation current" , doubles its value for every 10^0C rise in temperature.

Q.7. What are Zener diodes ? Explain its operation & characteristics. How a Zener diode can be used as a Voltage regulator ? [Important]

Related Short Answer Question

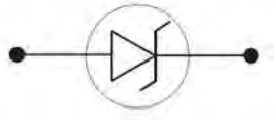
(i) What is zener diode ? Plot & explain its characteristics curve. [Kanpur 2013]

(ii) What is Zener diode ? How is Zener diode used as a voltage regulator in a power supply ? Explain. [Important]

(iii) What is a breakdoen diode (Zener diode). Discuss the origin of breakdown of a junction. [Important]

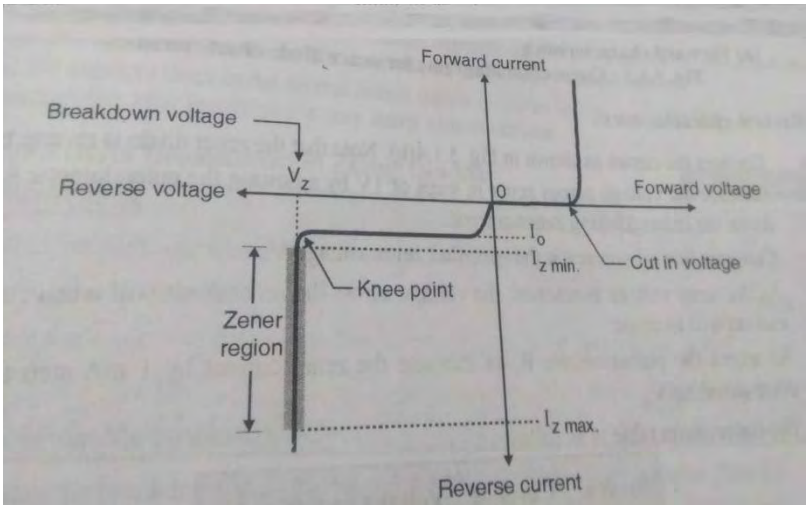
Zener Diode

Zener diode is a special type of p-n junction semiconductor diode that are designed to operate in the breakdown region



The V-I characteristics of Zener diode is a graph of voltage across the diode versus the current flowing through it .This characteristic is divided into two parts

1. Forward Characteristics 2. Reverse Characteristics



Forward Characteristics

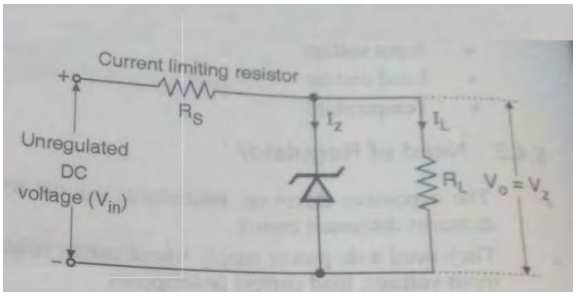
The Forward Characteristics of Zener diode is almost identical to forwar Characteristics of a p-n junction diode.

Reverse Characteristics

- The Reverse Characteristics of Zener diode is substantially different from that of the p-n junction diode.
- As we increase the reverse voltage , initially a small reverse saturation current "I_0" flows. This current flows due to thermally generated minority carriers.
- At a certain value of reverse voltage, the reverse current will increase suddenly and sharply. This is an indication that breakdown has occurred This breakdown is called as zener breakdown voltage or zener voltage denoted by V_Z.
- After breakdown , the voltage across the zener diode remains constant equal to V_Z
- The value of V_Z can be controlled by controlling the doping levels of p and n regions.

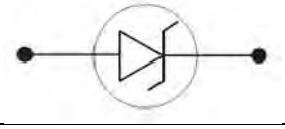
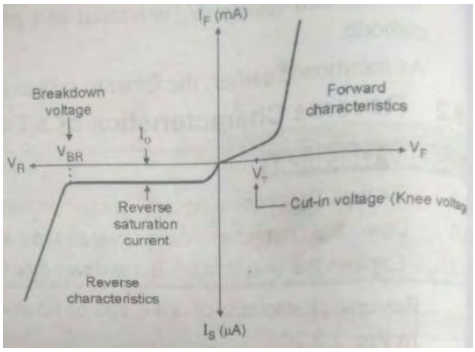
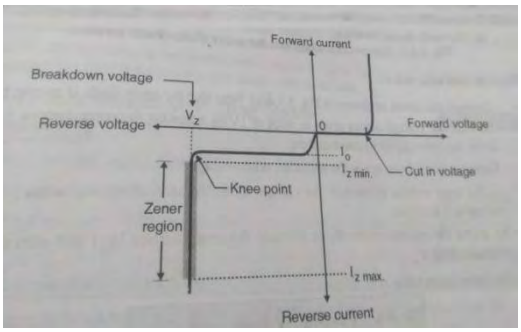
The Zener Voltage Regulator

The voltage across the zener diode remains constant equal to V_Z when it is operated in the "Zener region", this fact is utilized in Zener voltage regulator.



- If V_{in} ↑ then I ↑ , but I_L is constant as $I_L = \frac{V_Z}{R_Z}$
- Hence I_Z ↑ as $I_Z = I - I_L$
- If V_{in} ↓ then I ↓ , but I_L is constant
- Hence I_Z ↓ as $I_Z = I - I_L$

Q.8. Compare pn junction diode & Zener diode

S.No.	pn junction diode	Zener diode
1.	This is operated in the forward biased condition	Zener diode is normally operated in reverse bias condition.
2.		
3.		
4.	Applications: rectifiers, clipper, clamper, voltage multipliers etc	Applications: Voltage regulators, Voltage limiters etc.

Q.9. What do you understand by Zener & Avalanche breakdown? Distinguish between the two.

S.No.	Zener breakdown	Avalanche breakdown
1.	This is observed in zener diodes having V_Z between 4 to 6 volts	This is observed in zener diodes having V_Z above 6 volts.
2.	The valence electrons are pulled into conduction band due to intense electric field appearing across the narrow depletion region.	The valence electrons are pushed into conduction band due to the energy imparted by colliding accelerated minority carriers.
3.	The V-I Characteristics of Zener breakdown is vary sharp	The V-I Characteristics of Avelanche breakdown increases gradually . it is not as sharp as tzener breakdown.
4.	The breakdown voltage decreases with the increase in temperature.	The breakdown voltage increases with the increase in temperature.

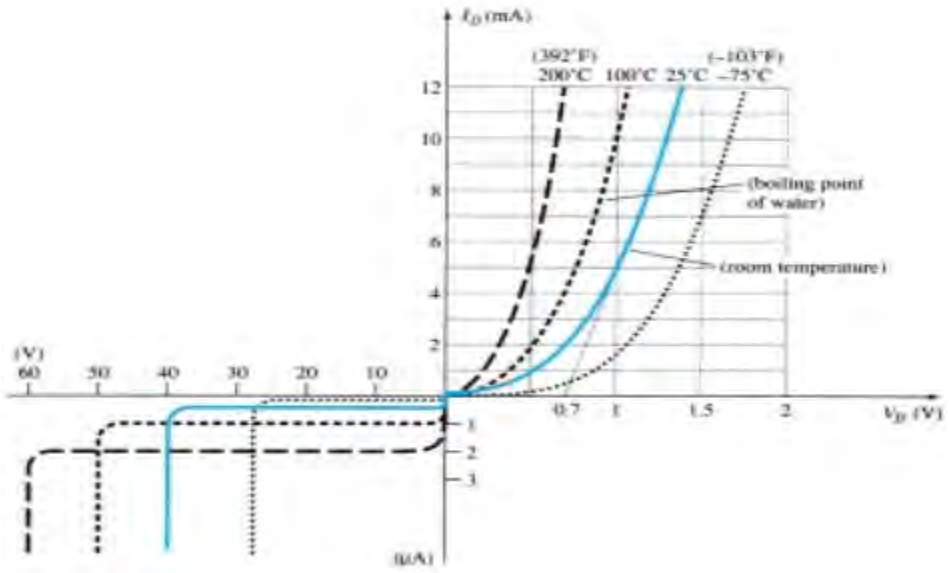
Q.10. What is Knee voltage of a diode ?Give its value for germanium and silicon diodes.

Ref. to Q.2

Q.11 Explain the effect of temperature on the temperature on the reverse saturation current in junction diode .

The diode characteristics is expressed by **Schockley equation** , $I= I_0[\exp(\frac{eV_T}{K_B T})-1]$

The parameters I_0 & V_T are temp. dependent



The forward characteristic of a si diode shifts to the left at a rate of 2.5mV per ^{0}C increase in temp.

In the reverse bias region , the reverse saturation current of a silicon diode doubles for every 10^0C rise in temperature.

The reverse breakdown voltage will increase or decrease depending on zener potential.

Q.12. What is a tunnel diode ? Explain its operation and working. Draw the characteristics of a tunnel diode and give its main use. [Important]

Or

What is a tunnel diode? Draw the volt-ampere characteristic curves of a such a diode. Explain the occurrence of a negative differential resistance in the characteristic. Mention some of its uses. [Important]

Or

Describe the construction and working of a tunnel diode. Sketch its V-I characteristics and explain. Mention its application. [Kanpur 2015]

Tunnel Diode

When the impurity is very high($\approx 10^{25}/m^3$) in both P and N-region of a P-N Junction diode , then the diode is known as tunnel diode. Since the barrier width of a diode is becomes very thin ($\approx 10^{-6}$cm) then, on applying forward bias voltage many carriers can tunnel through the depletion region known as tunneling. Hence the diode is known as tunnel diode.

No bias condition

Due to heavily doped, the fermi level lies within the bands of semiconductor at $T=0^0K$. Under no bias condition , the fermi level in the p side is at the same energy as the fermi level in N-side(fig. 1)AS the fermi level is the highest occupied energy level, so no current flows through the junction.

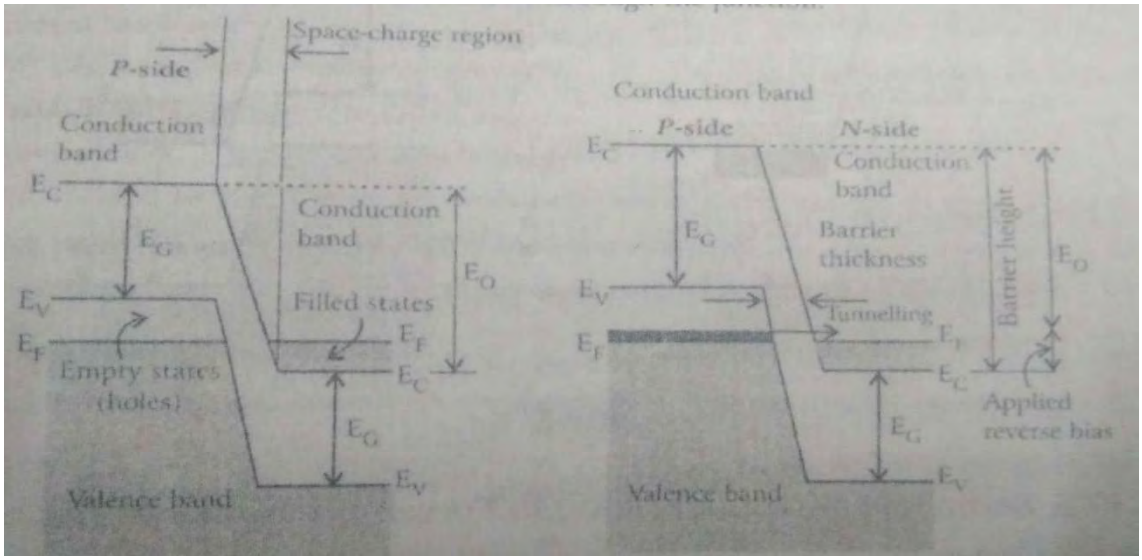


Fig. 1

Fig. 2

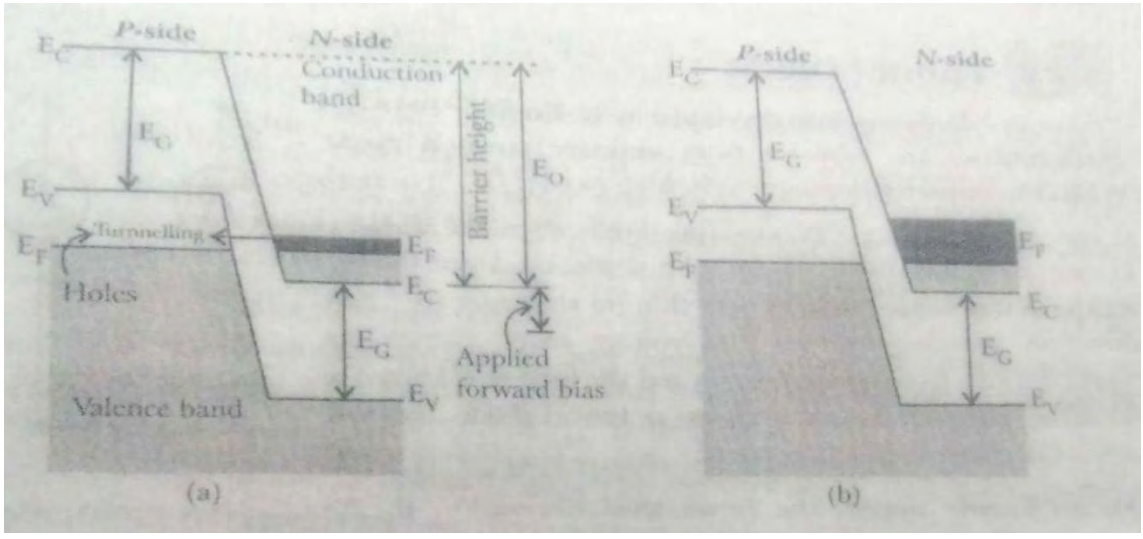
Reverse bias condition

On applying the reverse bias, the height of potential barrier is increased and the fermi level in the p- side goes up relative to that in N side(fig.2). The electrons in the valence band of p-side faces available unoccupied states at the same energy in the conduction band of N-side, across the barrier. Hence the electrons can tunnel from valence band of p-side to conduction band of N-side giving rise to reverse diode current.

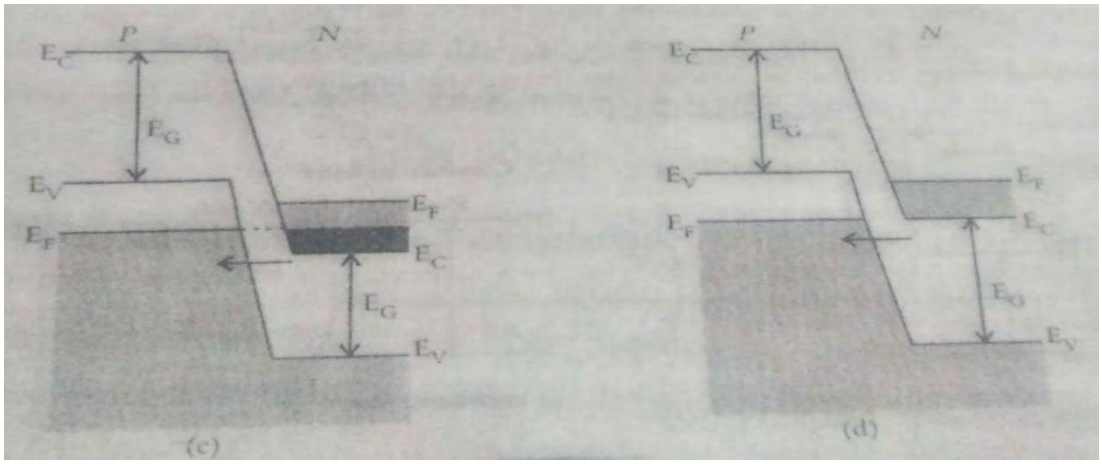
More the reverse bias, larger no. of electrons find available unoccupied sates on other side of thin barrier, as a result tunnel current increases with the reverse bias.

Forward bias condition

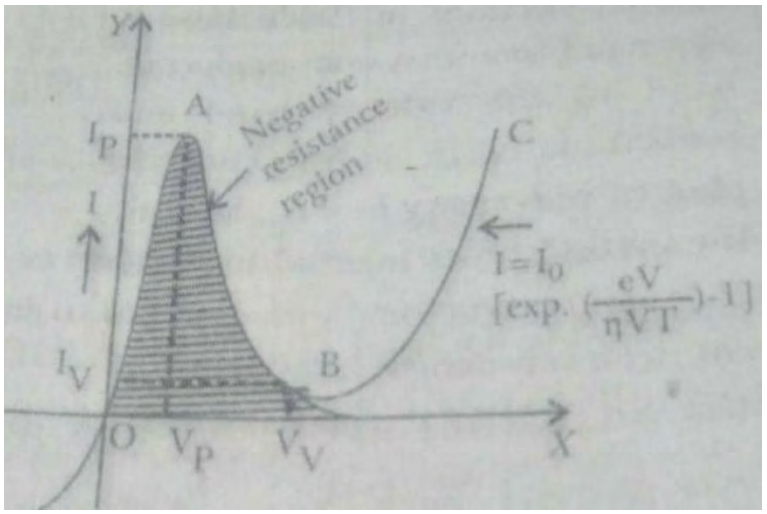
On applying forward bias , the height of potential barrier is decreased and the fermi level in the N-side moves up relative to that of p-side.[fig.(a)]. The electrons in the conduction band of N-side finds allowed empty energy states (holes) in valence band of p-side(at the same energy), across the barrier, Hence the electrons tunnel from N-side to p-side giving rise to large forward current.



On increasing the forward bias, maximum no. of electrons leave the occupied states in N-side & tunnel through the barrier to empty states in p-side, causing a peak current I_P to flow [fig.(b)]. On increasing the forward bias further, tunneling current decreases because available unoccupied states in p-side decreases[fig.(c)]. This corresponds to –ve resistance region AB of the V-I characteristics of tunnel diode. Finally for even larger forward bias, the energy band diagram is obtained as shown in [fig.(d)]



V-I Characteristics of Tunnel diode



The V-I characteristics of tunnel diode as shown in fig. The Portion OA of the characteristics is due to tunneling phenomenon.

If the forward voltage increases beyond V_P, current decreases and reaches to the minimum value I_V known as the valley current.

The forward bias voltage corresponding to valley current is known as valley voltage(V_V).

The tunnel diode posses –ve resistance b/w region AB. Above valley voltage , the tunnel diode behaves like an ordinary diode and the current increases exponentially with forward bias voltage.

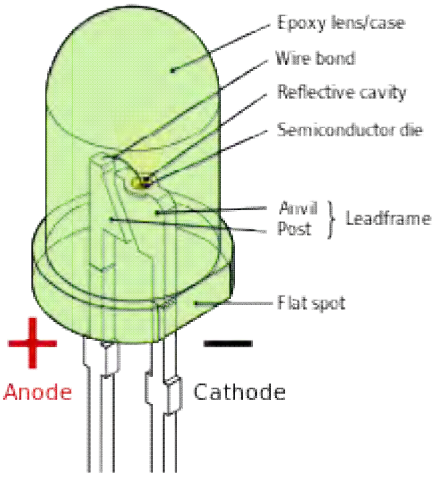
Q.13. Write short notes on :

(i) Solar cell. **(ii) L.E.D.**

Solar cell: A solar cell or photovoltaic cell, is an electrical device that converts the light energy into electrical energy by the photovoltaic effect, which is a physical and chemical phenomenon . Solar cells are the building blocks of solar panels.

They are used as a photo detector in optical communication.
The operation of a photovoltaic (PV) cell requires three basic attributes:

- The absorption of light, generating either electron-hole pairs or excitons.
- The separation of charge carriers of opposite types.
- The separate extraction of those carriers to an external circuit.



L.E.D.: L.E.D. i.e. light emitting diode is a p–n junction diode, which emits light when activated. When a suitable voltage is applied across the diode, electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence, and the color of the light (corresponding to the energy of the photon) is determined by the energy band gap of the semiconductor.
LEDs are now used in applications as diverse as aviation lighting, automotive headlamps, advertising, general lighting, traffic signals, camera flashes, and lighted wallpaper.

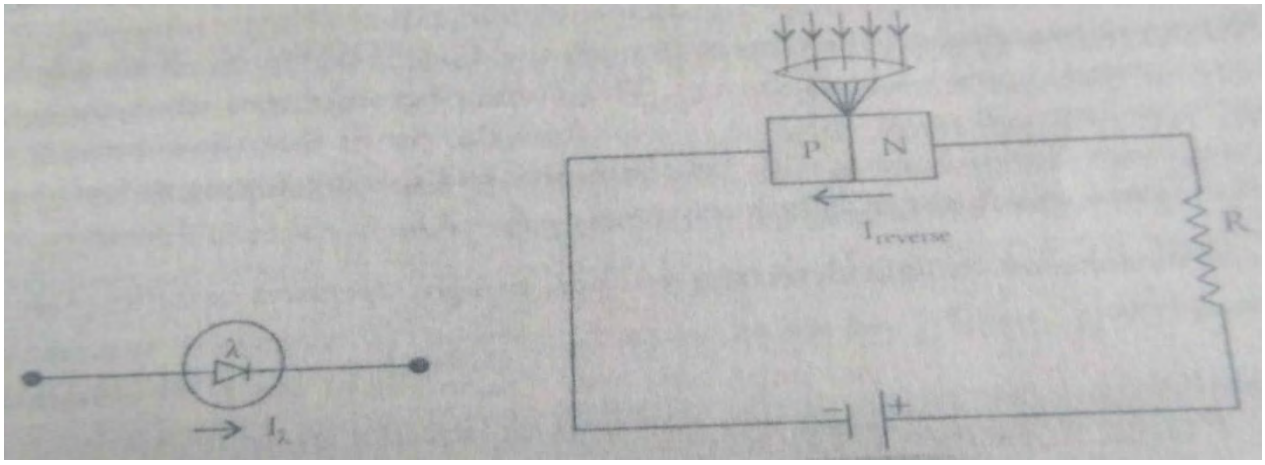
Q.14. Explain the working of photo diodes. **[Kanpur 2014]**

Or

Describe the construction and working of a photo diode. Give its characteristics.

[Kanpur 2016]

Photo diodeis a reverse baised P-N junction whose operation depends on the intensity of light fall on it . The symbol of photo diode is shown in fig.



In reverse biased P-N junction, a small reverse saturation current flows due to thermally generated holes & electrons (minority charge carriers) being swept across the junction, when there is no illumination.

Since there is no illumination or incident light , this reverse saturation current is known as **dark current,** In photodiode, the light energy dislodge valence electrons from their orbit as thermal energy dislodge valence electrons orbit as thermal energy dislodge valence electrons from their orbit on increasing the

junction temperature and generating more electron- hole pairs, this increase the reverse current flowing through the diode.

Further increase in the light intensity increase the reverse current. It means light intensity and reverse current are linearly related as shown in fig.(a)

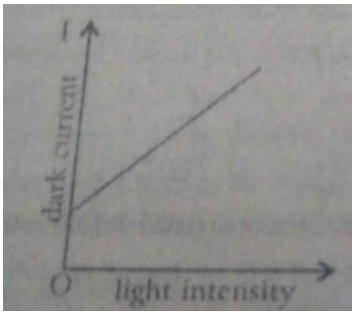


Fig. a

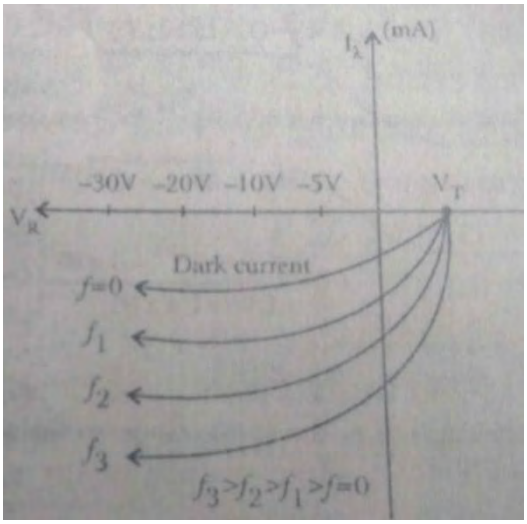


Fig. b

VI Characteristics

- The VI Characteristics shown in fig.(b) . It is a plot b/w current & reverse voltage for different illumination or light intensity (f). In the absence of illumination , the current through the diode is due to the thermally generated minority carriers, known as dark current.

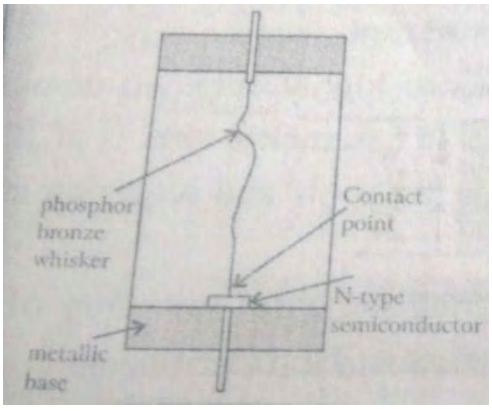
Dark current becomes zero when the applied voltage is positive and equal to V_T.

- From curve it is clear that the current through the diode varies almost linearly with light intensity and the spacing among different curve is equal for same increment in light intensity i.e. $f_2 = 2\ f_1$, $f_3 = 2f_2$ and so on.
- Photo diodes are used in light detection systems in light operated switches, tape, film, sound tracks etc.

Q.16. What is point contact diode? Discuss its working & uses at high frequencies. [Kanpur 2014]

Or

Explain the construction and working of point contact diode. Mention its application at high frequencies. [Kanpur 2016]

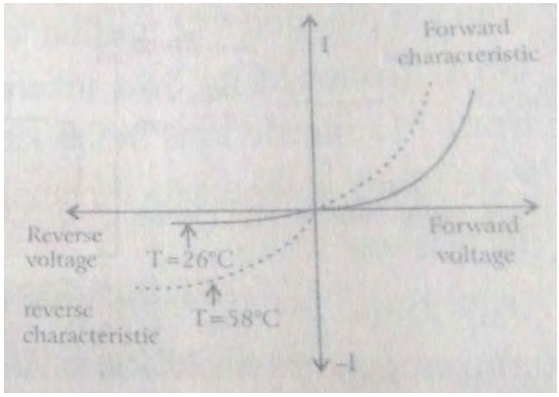


Point Contact diode is a small wafer of a semiconductor crystal having an area of few square millimeters and a thickness of a fraction of mm. The crystal is soldered to a metallic base so that an external ohmic contact can be made.

The point contact is made by pressing phosphorous bronze wire (called cat wisker) against the exposed surface of semiconductor crystal. In case of N-type semiconductor , the forward current flows from the phosphor bronze wire to the semiconductor.

The operation of the diode depends on the pressure of contact between a point and a semiconductor crystal.

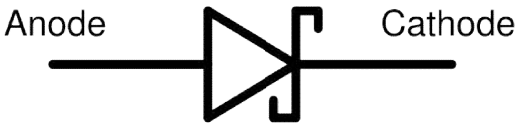
The **V-I characteristics** curve of the point contact diode for two different temperature T=26^{0}C & 58^{0}C is shown in fig.



Point contact diode is very useful for the operation at high frequencies (≈10KHz) and in pulse circuits in contrast to normal diode.

Q.17. What is Schottky diode ? Why Schottky diode is known as hot carrier diode? How it differs in construction from a normal P- N junction ? Give its working , characteristics and applications.

As frequency increases , the action of normal diodes begins to deteriorate as a rectifier. They are no longer able to switch off fast enough to produce a well-defined rectified signal. The solution for this problem is the schottky diode.



The symbol shown in figure, the cathode side looks like a rectangular S, which stands for schottky diode.

Differ from normal diode

It is a semiconductor diode formed by the junction of a semiconductor with a metal. This diode uses a metal such as gold, silver, or platinum on one side of the junction and doped silicon (typically n-type) on the other side.

Diode Biasing

When the schottky diode is unbiased, free electrons on the n-side are in smaller orbits then the free electrons on the metal side. This difference in orbit size is called the **Schottky barrier**, approximately 0.25V.

When the diode is forward bias, free electrons on the n side can gain enough energy to travel in larger orbits, because of this electrons cross the junction and enter the metal , producing a large forward current. Since the metal has no holes, there is no charge storage and no reverse recovery time.

Hot carrier diode

Schottky diode is called as a hot carrier diode , this name came as follows . Forward bias increases the energy of the electrons on the n-side to a higher level then that of electron on the metal side of the junction. This increase in energy inspired the name hot carrier for the n-side electrons.

As soon as these high- energy electrons cross the junction , they fall into the metal, which has a lower-energy conduction band.

High- Speed Turnoff

Due to lack of charge storage schottky diode can be turned off faster than the normal diode. Because this property , the diode is used to rectify frequencies above 300MHz.

Applications

- Used in RF mixer and Detector diode
- Used in high power rectifier.
- Used in Solar cell applications
- Schottky barrier diodes may also be used as a clamp diode in a transistor circuit to speed the operation when used as a switch.

Q.18. What is thermistors? Give its construction, working and applications. [Important]

A thermistor is a type of resistor whose resistance strongly depends on temperature. The word thermistor is a combination of words "thermal" and "resistor". Thermistors are available in various shapes like disc, rod, washer, bead etc as shown in fig.(a).

A thermistor is a temperature-sensing element composed of sintered semiconductor material and sometimes mixture of metallic oxides such as Mn, Ni, Co, Cu and Fe, which exhibits a large change in resistance proportional to a small change in temperature.

Pure metals have positive temperature coefficient of resistance, alloys have ≈ zero temperature coefficient of resistance and semi conductors have negative temperature coefficient of resistance.

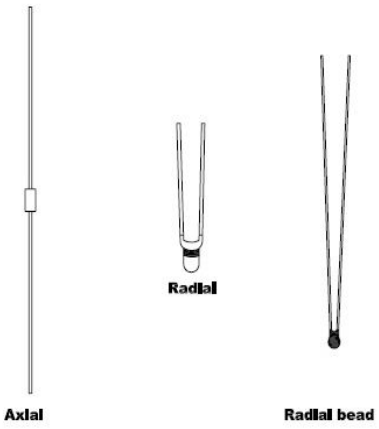


Fig. a

Thermistors can be classified into two types:

- Positive temperature coefficient (PTC) thermistor:-resistance increase with increase in temperature.
- Negative temperature coefficient (NTC) thermistor:- resistance decrease with increase in temperature.

The thermistor exhibits a highly non-linear characteristic of resistance vs. temperature.

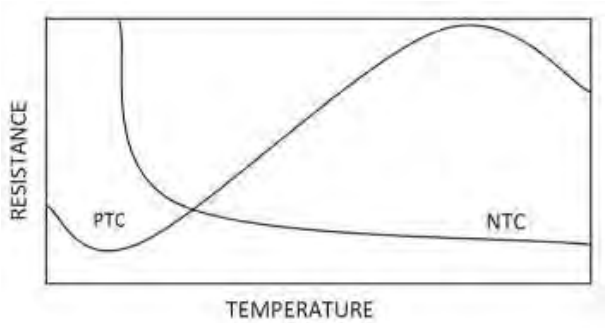


Fig. b

PTC thermistors can be used as heating elements in small temperature controlled ovens. NTC thermistors can be used as inrush current limiting devices in power supply circuits. Inrush current refers to maximum, instantaneous input current drawn by an electrical device when first turned on.

Applications

- PTC thermistors were used as timers in the degaussing coil circuit of most CRT displays. A degaussing circuit using a PTC thermistor is simple, reliable (for its simplicity), and inexpensive.
- PTC thermistors are used as heater in automotive industry to provide additional heat inside cabin with diesel engine or to heat diesel in cold climatic conditions before engine injection.
- PTC thermistors is used as current-limiting devices for circuit protection, as replacements for fuses.
- NTC thermistors is used to monitor the temperature of an incubator.

- Thermistors are also commonly used in modern digital thermostats and to monitor the temperature of battery packs while charging.
- We regularly use NTC thermistors in automotive applications.
- NTC thermistors are used in the Food Handling and Processing industry, especially for food storage systems and food preparation. Maintaining the correct temperature is critical to prevent food borne illness.
- NTC thermistors are used throughout the Consumer Appliance industry for measuring temperature. Toasters, coffee makers, refrigerators, freezers, hair dryers, etc. all rely on thermistors for proper temperature control.
- We can regularly use the Thermistors in the hot ends of 3D printers; they monitor the heat produced and allow the printer's control circuitry to keep a constant temperature for melting the plastic filament.
- NTC thermistors are used as resistance thermometers in low-temperature measurements of the order of 10 K.
- NTC thermistors can be used as inrush-current limiting devices in power supply circuits.

Numerical

Q.1. When a silicon diode having a doping concentration of $N_A = 9 \times 10^{16}$ cm^{-3} on p-side and $N_D = 1 \times 10^{16}$ cm^{-3} on n-side is reverse biased, the total depletion width is found to be 3 µm. Given that the permittivity of silicon is 1.04×10^{-12} F/cm, find the depletion width on the p-side and the maximum electric field in the depletion region. [Important]

Exp: Given $N_A = 9 \times 10^{16}$ / cm^3 ; $N_D = 1 \times 10^{16}$ / cm^3

Total depletion width, $x = x_n + x_p = 3$ µm.

$$\epsilon = 1.04 \times 10^{-12} \text{ F / cm}$$

Since $\frac{X_n}{X_p} = \frac{N_A}{N_D} = (9 \times 10^{16})/(1 \times 10^{16})$

$$X_n = 9X_p$$

$\because x = x_n + x_p = 3$ µm.

$9 x_p + x_p = 3$ µm.

$\therefore x_p = 0.3$ µm

Max. Electric field, $E = qN_AN_D / \epsilon = (1.6 * 10^{-19} * 9 \times 10^{16} * 1 \times 10^{16}) / (1.04 \times 10^{-12})$

$$= 4.15 \times 10^5 \text{ V / cm Ans}$$

Q.2. A diode has a power rating of 5W. if the diode voltage is 1.2 V and the diode current is 17.5 A, what is the power dissipation ? will the diode be destroyed ?

Exp: $\because P_D = V_D I_D$

$\therefore P_D = (1.2V)(1.75A) = 2.1W$

$\because P_D < 5W$ so the diode will not destroyed.

Q.3. Find the dynamic resistance of a P-N junction diode at a forward current of 2mA. Assume kT/q= 25mV.

Exp: Given , forward current = 2mA= 0.002A

Volt equivalent of temp. , V_T= **kT/q= 25mV**

$\because$ Dyamic resistance (r) = $\eta V_T / I$ (η=1)

$\therefore r = 0.025/0.002 = 12.5\ \Omega$.

Q.4. Assuming the barrier potential of 0.7V at an ambient temperature of 25^{0}C , What is the barrier potential of a silicon diode whwn the junction temperature is 100^{0}C ? At 0^{0}C ?

Exp: When the Junction temp. is 100^0C , the change in barrier potential is

$\Delta V = (-2.5mV/^0C)\,\Delta T = (-2.5mV/^0C)(\mathbf{100^0C - 25^0C}) = -187.5mV$

$\therefore$ The barrier potential will decrese by 187.5mV

i.e. $V_B = 0.7V - 0.18V = 0.52$ V Ans

When the Junction temp. is 0^0C , the change in barrier potential is

$\Delta V = (-2.5mV/^0C)\,\Delta T = (-2.5mV/^0C)(\mathbf{0^0C - 25^0C}) = 62.5mV$

$\therefore$ The barrier potential will increase by 62.5mV

i.e. $V_B = 0.7V = 0.0625 = 0.7625$ V Ans

Q.5. A Silicon diode has a saturaration current of 5nA at 25^0C . What is the saturation current at 100^0C ?

Exp: The change in temp

$\therefore \Delta T = 100^0C - 25^0C = 75\ ^0C$

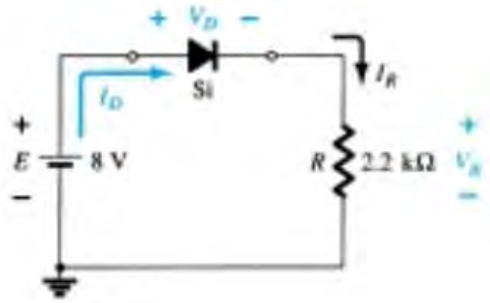
$\because$ there is seven doubling between 25^0C to 95 ^{0}C

$\therefore \quad I_S = (2^7)(5nA) = 640nA$

$\because$ there is 5 ^{0}C rise in temp from 95^0C to 100 ^{0}C

$\therefore \quad I_S = (1.07^5)(640nA) = 898nA$ Ans

Q.6. For the series diode configuration determine V_D, V_R and I_D.



Exp: $\because$ Diode is of silicon type therefore $V_D = 0.7V$

$V_R = (8-0.7)V/2.2K\Omega$

$= 7.3V/2.2K\Omega$

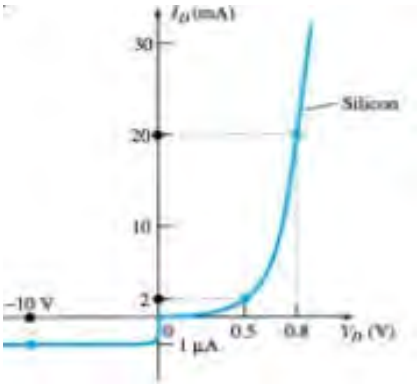
$= 3.32mA$ Ans

Q.7. Determine the dc reistance levels for the diode shown in fig. at

(a) $I_D = 2mA$

(b) $I_D = 20mA$

(c) $V_D = -10V$



Exp: (a) At $I_D = 2mA$, $V_D = 0.5\ v$(from the curve)

$\therefore R_D = V_D/I_D = 0.5v/2mA = 250\ \Omega$ Ans

(b) At $I_D = 20mA$, $V_D = 0.8\ v$(from the curve)

$\therefore R_D = V_D/I_D = 0.8v/20mA = 40\ \Omega$ Ans

(c) At $V_D = -10V$, $I_D = -1\mu A$ (from the curve)

$\therefore R_D = V_D/I_D = -10v/-1\mu A = 10\ M\Omega$ Ans

Q.8. The current through p-n junction is 50mA at a forward bias voltage of 3.0volt. At temp. 27^0C , find the static and dynamic resistance of the diode. [Kanpur 2012, Important]

Exp: Given V=3V, I=50mA

Static resistance is given as $R_{dc} = V/I$

$\therefore R_{dc} = 3/50mA$

$= 60\ \Omega$ Ans

Dynamic resistance is given as $r_{ac}=\frac{dV}{dI}$

$\because I = I_0[\exp(\frac{eV}{\eta K_B T})-1] \quad = I_0[\exp(\frac{V}{\eta V_T})-1]$

Here V_T= 0.026V=26mV, I= 50mA

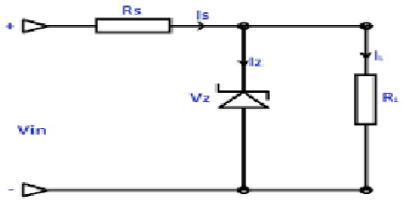
for silicon η= 1 ,$r_{ac}= \eta V_T / I$ = 26mV/50mA= 0.52 Ω Ans

Q.9. Calculate the value of

(i) Voltage difference across series resistance.

(ii) Electric current in zener diode. **[Important]**

Given V_{in}= 100V , V_Z= 60V , R_S = 5KΩ , R_L= 10KΩ



Exp: Given V_{in}= 100V , V_Z=60V, R_S = 5KΩ , R_L= 10KΩ

(i) Then V_S(voltage across R_S) = (100-60) V= 40V Ans

(ii) I_S= 40V/ 5KΩ = 8mA

$I_L= V_Z/ R_L$ = 60V/10 K Ω= 6mA

$\because I_S = I_Z + I_L$

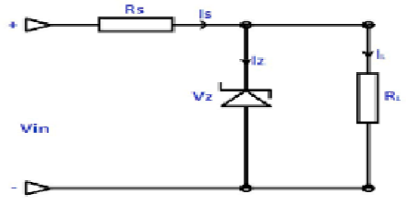
$\therefore I_Z$ = (8-6)mA= 2mA Ans.

Q.10. For the following circuit find:

(i) Output voltage (ii) Voltage drop across R_S (iii) Current through the zener diode

Given V_{in}= 120 V , V_Z= 50V , R_S = 5KΩ , R_L= 10KΩ

[Important]



Exp: Given V_{in}= 120V , V_Z=50V, R_S = 5KΩ , R_L= 10KΩ

(i) Since zener diodes breakdown takes place

$\therefore$ Output Voltage = V_Z= 50V Ans.

(ii) V_S(voltage across R_S) = (120-50) V= 70V Ans

(iii) I_S= 70V/ 5KΩ = 14mA

$I_L= V_Z/ R_L$ = 50V/10 K Ω= 5mA

$\because I_S = I_Z + I_L$

$\therefore I_Z$ = (14-5)mA= 9mA Ans.

Q.11. Maximum 20mA current can flow through a zener diode . If Zener voltage is 6volt, how much resistance will have to be applied in series with the zener diode for 9 volt supply? Calculate load current & zener current if load resistance is of 1 KΩ. **[Kanpur 2014,16]**

Part –I Exp: Given V_{in}= 9V , V_Z=6V, I_Z= 20mA, R_S = ?

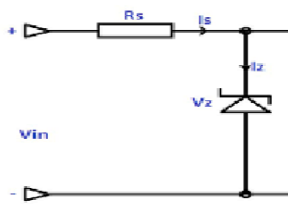
$\because I_Z$= 20mA, & the zener diode is in series of R_S

It means 20mA current will also flow through R_S

Here V_S= (9-6)V= 3V

I_S= 20mA

$\therefore R_S$ = 3V/20mA= 150 Ω Ans

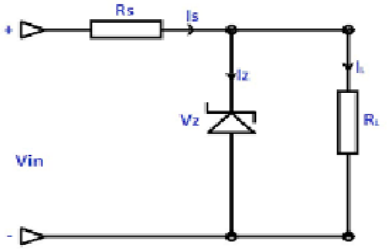


Part –II

Exp: Given V_{in}= 9V , V_Z=6V, V_S= 3V ,

R_S = 150 Ω,

R_L= 1K Ω , I_Z= ?, I_L=?



$\because$ V_S= 3V

$\therefore$ I_S= 3V/ 150 Ω= 20mA

$\therefore$ I_L= 6V/ 1K Ω = 6mA

$\because$ $I_S = I_Z + I_L$

$\therefore$ I_Z = (20-6)mA= 14mA Ans

Q.12. A zener regulator has Vz=15V. The input voltage may vary from 22 to 40volt and load current from 20 to 100mA. To hold load voltage constant under all conditions, what should be the value of series resistance? [Kanpur 2011, Important]

Exp: Given V_{in}= 15V,

δV_i= (40-22)V= 18V

δI_L=(100-20)mA= 80mA

$\because$ $\delta V_i = R\ \delta I_L$

$\therefore$ R= 18/(8x 10^{-2})= 225 Ω

Q.13. A LED is made of gallium phosphide for which the band gap energy E_g= 2.26eV, at room temperature.Find the wavelength of light emitted by it when it is forward biased.

[Kanpur 2015]

Exp: Given E_g=2.26eV=2.26 x1.6x10^{-19} Joule

h=6.62 x 10^{-34}, c=3x10^8m/s

$\because$ The wavelength of the emitted light is given as $\lambda = h_c/E_g$

$\therefore$ λ= 6.62 x 10^{-34}/3x10^8 =5.49x 10^{-7}

= 5490 Å Ans

Chapter-3
Bipolar Junction Transistor

The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an npn transistor, while the latter is called a pnp transistor.

The unbiased transistor

A Transistor has three doped regions: an emitter , a base and the collector. A p-n junction exists between the base and the collector; this part of transistor is called the emitter diode. Another p-n junction exists between the base and the collector; this part of the transistor is called the collector diode.

The Biased Transistor

For the normal operation, we forward bias the emitter diode & reverse bias the collector diode . Under these conditions the emitter sends free electrons into the base. Most of these free electrons pass through the base to collector. Because of this, the collector current approximately equal the emitter current. The base current is much smaller ≈ 5% of emitter current.

Transistor Current

The ratio of the collector current to the base current is called the current gain symbolized as β_{dc} or h_{FE}, For low-power transistor, this is typically 100 to 300. The emitter current is the largest of the three currents, the collector current is almost as large and the base current is much smaller.

The CE Configuration

The emitter is grounded or common in CE circuit. The base-emitter part of a transistor acts approximately like ordinary diode. The base-collector part acts like a current source that is equal to β_{dc} times the base current. The transistor has an active region , a saturation region and a breakdown region. The active region is used in linear amplifier, Saturation and cutoff are used in digital circuits (as a switch).

Collector curves

The four distinct operating region, are the active region, the saturating region , the cut off region & the breakdown region . When it is used as an amplifier, the transistor operates in the active region. When it is used in digital circuits, the transistor operates in the saturation & cutoff region. The breakdown region is avoided because the risk of transistor destruction is too high.

The Load line

The dc load line contains all the possible dc operating points of a transistor circuit. The upper end of the load line is called saturation and the lower end is called cutoff. Saturation conditions arises a short b/w collector & emitter and the cutoff condition arises open b/w collector & emitter.

The Operating Point

The operating point of transistor is on the dc line. The exact location of this point is determine by the collector current & the collector-emitter voltage.

Current amplification factor in C-E Mode (β):

The current amplification factor or current gain in C-E mode is defined as the ratio of the change in the collector current (ΔI_C) to the change in base current (ΔI_B) at a constant collector-emitter voltage (V_{CE})
It has a value between 20 to 500.

Current amplification factor in C-B Mode(α):

Defined as the ratio of the change in the collector current (ΔI_C) to the change in emitter current (ΔI_E) at a constant base- collector voltage (V_{CB}). The value of $\boldsymbol{\alpha}$ in general is slightly lesser then unity.

Base width modulation

As the collector to emitter voltage V_{CC} is made to increase the reverse bias , the space charge width between collector and base tends to increase, with the result that the effective width or the base decreases. This dependency of base width on collector to emitter voltage is known as the base width modulation or early effect.

Transit time & life time of minority carriers

To have a good p-n-p transistor , we prefer that almost all holes injected by the emitter into the base be collected. Thus n-type base region should be narrow & the hole life time t_p should be long i.e. $W_b << L_p$, where W_b is the length of the neutral n-type material & L_p is the diffusion length.

There is an important difference in the times which electrons & holes spend in the base. The average excess hole spends a time $\tau_{p,}$ defined as the **transit time from emitter to collector.**

Life time of Minority Carriers

Carrier lifetime is defined as the average time it takes for a minority carrier to recombine. Carrier lifetime plays an important role in bipolar transistors and solar cells.

Base emitter resistance

Base Emitter Resistance is a resistance that provides the required amount of automatic biasing needed for a common emitter amplifier

Base spreading resistance

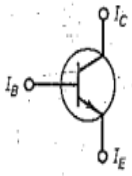
Resistance which is found in the base of any transistor and acts in series with it, generally a few ohms in value known as base spreading resistance

Diffusion Capacitance

When the p-n junction diode is forward biased, a capacitance which is much larger then the transient capacitance is known as diffusion capacitance (C_D) or storage capacitance.

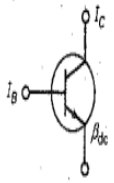
Derivations :

Emitter current



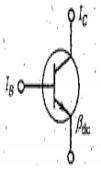
$I_E=I_C+I_B$

Collector Current



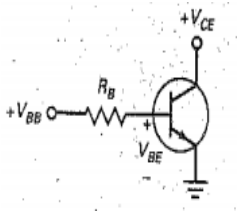
$I_C= \beta I_B$

Base Current



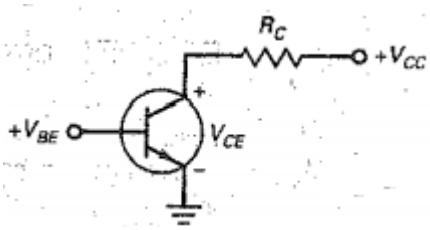
$I_B= I_C/ \ \beta_{dc}$

Base current



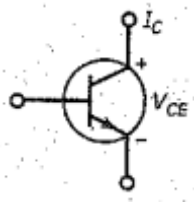
$I_B=(V_{BB}-V_{BE})/ R_B$

Collector- emitter Voltage



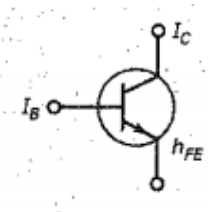
$V_{CE}=V_{CC} -I_CR_C$

CE power dissipation

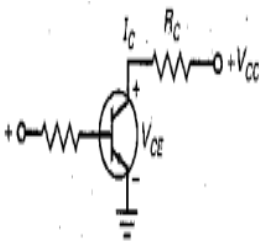


$P_D=V_{CE} I_C$

Current gain



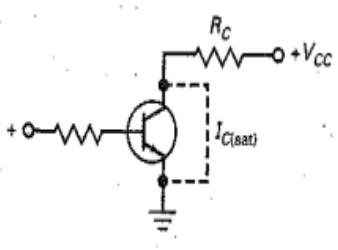
$\beta_{dc}=h_{FE}$



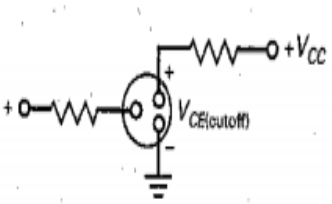
Load line analysis

Saturation Current

$I_C=(V_{CC}-V_{CE})/\ R_CI_{C(sat)}$
$I_C(sat)= V_{CC}/R_C$

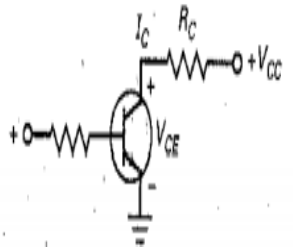


Cutoff Voltage (base bias)



$V_{CE(cutoff)}=V_{CC}$

Emitter voltage



$V_{CE=}V_{CC} - I_CR_C$

Long & Short Questions

Q.1. Define BJT , Why BJT is called bipolar? Describe its operating regions.

Transistor

A transistor is a three terminal solid state device, whose operation depends upon the flow of charge carrier with in solid. BJT is formed by sandwiching one type of semiconductor (p-type or n-type) between two layers of other types , creating three terminals

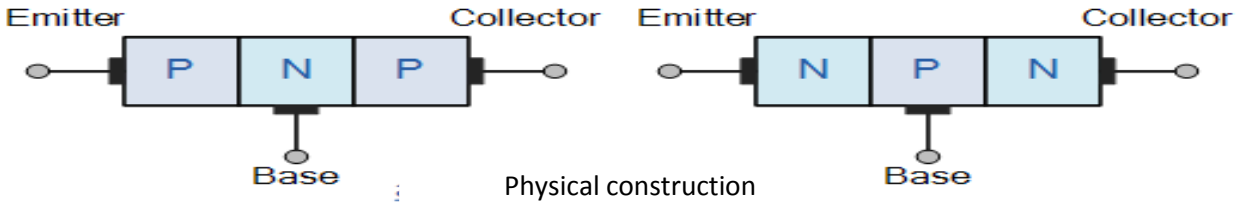
The three terminals are Emitter (E) , Base(B) & Collector(C)

Emitter: It is a terminal through which charge carriers enters in base . It is quite large in compare to base

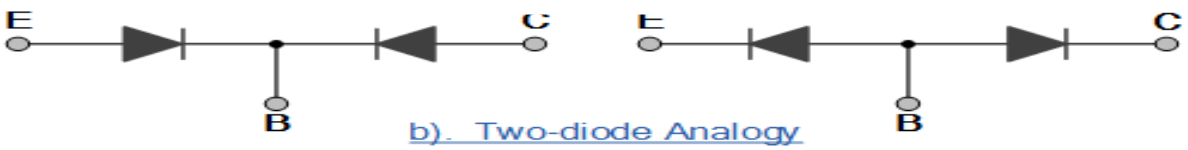
Base : It is a terminal through which charge carriers(electrons or holes) enters in collector, it is very small.

Collector : It is the largest terminal charge carriers coming from base collect here, therefore to reduce energy dissipation it is made so large.

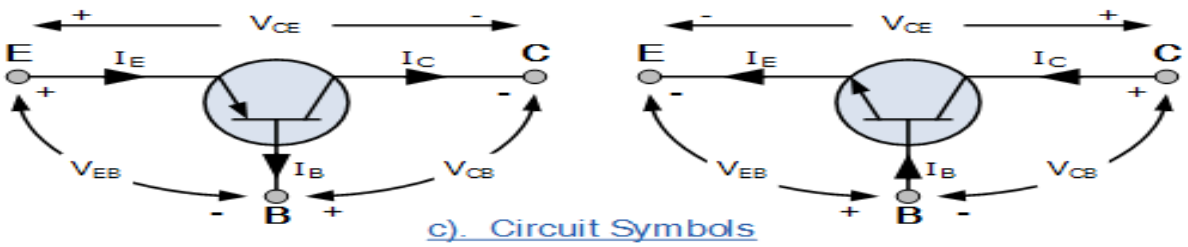
Transistor has two types of physical construction , two diode analogy & circuits symbols are as shown in fig. below :



Physical construction



b). Two-diode Analogy



c). Circuit Symbols

In order to distinguish the emitter & collector an arrow is included in the emitter. The direction of arrow depends on the flow of conventional current, when the emitter base junction is forward bias.

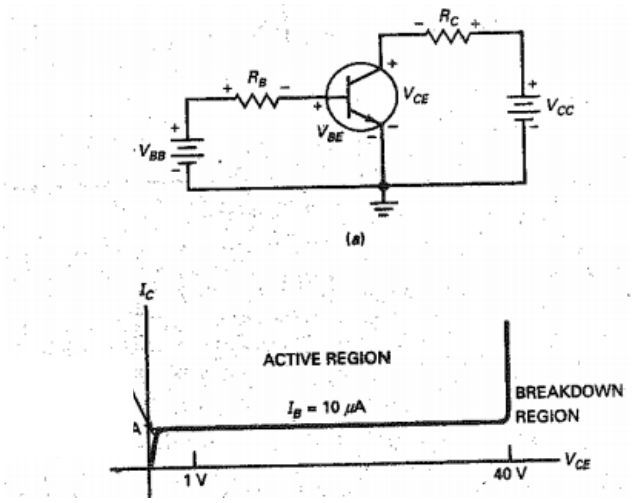
Bipolar

Transistor operation is carried out by two types of charge carrier i.e. electrons & holes, because of this the transistor is known bipolar .

BJT operating regions

The transistor can operate in different regions as Active, Breakdown & Saturation

Active region : It is a region (
collector voltage have no effe(
i.e. collector current acts as a current source. It occurs when emitter base junction is forward bias & Collector base junction is reversed bias.



Circuit Symbols

Breakdown region : It is a region in which current through the BJT is ≈ zero i.e. off state of diode.

It occurs when emitter base junction is reverse bias & Collector base junction is reversed bias.

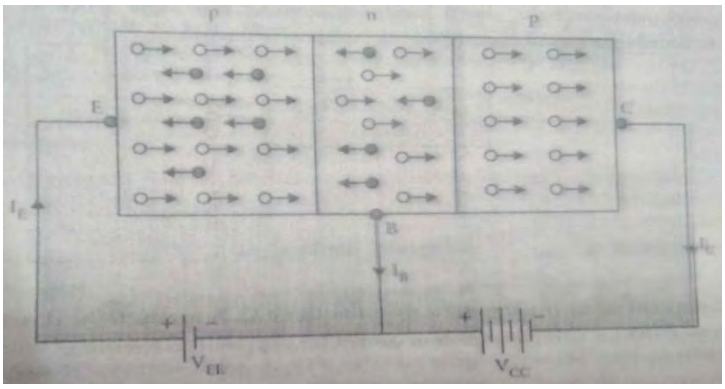
Saturation region :When emitter base junction & Collector base junction both are made forward bias,

BJT enters into region known as Saturation region. In this region V_{CE} is between 0V to 0.3 V.

Q.2. Explain the mechanism of current flow in NPN & PNP transistors. [Important]

Mechanism of current flow in NPN transistor

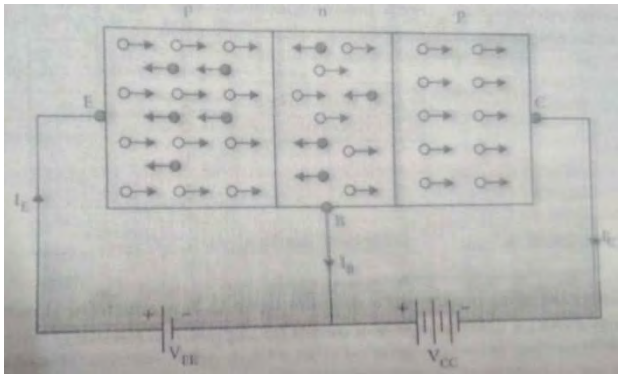
The operation of n-p-n transistor is shown in fig. Forward bias is provided to emitter base junction & reverse bias is provided to base-collector junction.



- Under the forward biasing of B-E junctions the electrons of emitter (n-region) moves toward base(p-region) and holes of the p-region moves towards emitter.
- As the base is very thin , nearly 95% to 98% electrons crosses the base and enters in to collectors region while remaining recombines with holes in p-region.
- Electrons entering the collectors region under the influence of reverse bias , are attracted towards the collector terminal.
- As the electron reach the terminal C, enters the +ve terminal of battery V_{CC} , an electron from the –ve terminal of battery V_{EE} enters the emitter which compensate the loop of electron.
- Thus for a transistor , we can say that , $I_E = I_B + I_C$, where I_E , I_B, &I_C are emitter current , base current & collector current respectively.

Mechanism of current flow in PNP transistor

The operation of p-n-p transistor is shown in fig. As the small forward bias is provided to emitter- base(p-n) junction and reverse bias to base-collector(n-p) junction.



- Under the forward biasing of B-E junctions the holes (+vely charged) in the emitter(p-region) move towards the base, while electrons(-vely charged) in the base(n-region) move toward emitter.
- As the base is very thin, 95% to 98% entering it passes on to the collector, & remaining combines with the electrons present in the base.
- Holes entering the collector move under the reverse bias voltage which helps them to pull towards the collector terminal C.
- As the hole reach the terminal C, they combine with the electrons coming from the –ve terminal of battery V_{CC} and both electron & holes neutralized each other.
- Thus $I_E = I_B + I_C$, where I_E , I_B, &I_C are emitter current , base current & collector current respectively.

Q.3. Define α & β and derive the relationship between them.

Current amplification factor in C-B Mode(α):

Defined as the ratio of the change in the collector current (ΔI_C) to the change in emitter current (ΔI_E) at a constant base- collector voltage (V_{CB}).

$\therefore \boldsymbol{\alpha} = \Delta I_C / \Delta I_E$ at V_{CB}= constant

The value of **α** in general is slightly lesser then unity.

Current amplification factor in C-E Mode (β):

The current amplification factor or current gain in C-E mode is defined as the ratio of the change in the collector current (ΔI_C) to the change in base current (ΔI_B) at a constant collector-emitter voltage (V_{CE})

$\therefore \beta = \Delta I_C / \Delta I_B$ at V_{CE}= constant

It has a value between 20 to 500.

Relationship between α & β

$\because I_E = I_B + I_C$

Dividing throughout by I_C

We have $I_E / I_C = I_B / I_C + 1$

$\Delta I_E / \Delta I_C = \Delta I_B / \Delta I_C + 1$

$\therefore 1/\alpha = 1/\beta + 1$

Q.4. Define the term reverse saturation current & its relation.

The collector current I_C of the common base configuration is given by

$I_C = I_{C(INJ)} + I_{CBO}$

$I_{C(INJ)}$: It is called as the injected collector current & due to the no. of electrons crossing the collector base junction. $I_{C(INJ)} = \alpha . I_E$

I_{CBO} : This is reverse saturation current flowing due to minority carriers between collector & base when emitter is open. **I_{CBO}** is negligible as compare to $I_{C(INJ)}$.

Q.4. Derive the relation $I_C = \beta I_B + (1+\beta) I_{CO}$

For the CE configuration we have $I_E = I_B + I_C$ Where $I_C = \alpha . I_E + I_{CBO}$

Rearranging the above equations we have

$I_C - I_{CBO} = \alpha . I_E = \alpha(I_B + I_C)$

$\Rightarrow I_C(1-\alpha) = I_{CBO} + \alpha I_B$

$\Rightarrow I_C = I_B(\frac{\alpha}{1-\alpha}) + I_{CBO}(\frac{1}{1-\alpha})$

$\Rightarrow I_C = I_B.\beta + I_{CBO}(\frac{1}{1-\alpha})$ $\quad \{\because \beta = \frac{\alpha}{1-\alpha}\}$

$\because \beta = \frac{\alpha}{1-\alpha}$

Adding both side 1 , we have

$\because \beta+1 = \frac{\alpha}{1-\alpha} + 1 \Rightarrow \beta+1 = \frac{1}{1-\alpha}$

$\therefore \quad I_C = I_B.\beta + I_{CBO}(\frac{1}{1-\alpha})$

$I_C = I_B.\beta + I_{CBO}(\beta+1)$ Hence Proved

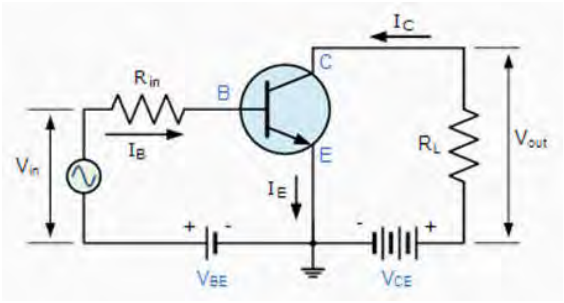
Q.5. Draw circuit diagram of common emitter transistor amplifier & explain its working .

[Important]

Or

Draw a circuit diagram & explain the method of obtaining the characteristics curves of a n-p-n transistor in common emitter configuration and obtain the relation between between current gain for common base & common emitter configuration in a transistor.

[Important]



Common emitter transistor

The input signal is applied across the base and emitter terminal while output is taken across collector & emitter with the help of load resistance R_L.

This is the most flexible & efficient configuration in compare to other configuration. In this configuration the collector current is controlled by base current only.

Characteristics curves of transistor in C-E Mode:

A n-p-n common emitter configuration is shown in fig. This configuration is most widely used because of high amplification .

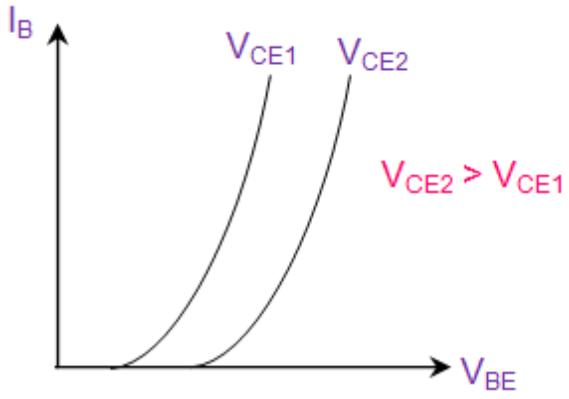


Fig. (a) Input Characteristics

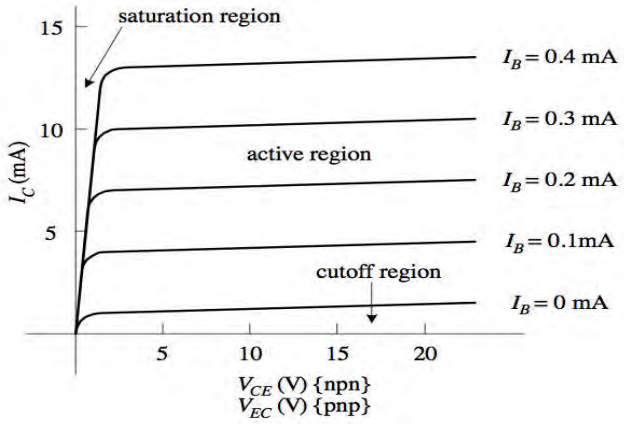


Fig. (b) Output Characteristics

Input Characteristics

In order to obtain the input characteristics of C-E Mode as shown in fig., for the collector – emitter voltage V_{CE} at V_{CE1} and increase in voltage V_{BE} leads to increase in base current (I_B).The process is repeated for different values of $V_{CE,}$ then I_B is plotted as a function of V_{BE}. This is known as input characteristics.

Output Characteristics

To obtain the output characteristics of a n-p-n transistor in CE mode , keeping V_{BE} & I_B constant , V_{CE} is increased & I_C is obtained . The plot between I_C & V_{CE} for the given V_{BE} & I_B known as Output Characteristics as shown in fig. (b).

In this characteristics there are three regions of operations i.e. Active, Saturation & Cutoff region.

Current amplification factor in C-E Mode (β):

The current amplification factor or current gain in C-E mode is defined as the ratio of the change in the collector current (ΔI_C) to the change in base current (ΔI_B) at a constant collector-emitter voltage (V_{CE})

$\therefore \beta = \Delta I_C / \Delta I_B$ at V_{CE}= constant

It has a value between 20 to 500.

Current amplification factor in C-B Mode(α):

Defined as the ratio of the change in the collector current (ΔI_C) to the change in emitter current (ΔI_E) at a constant base- collector voltage (V_{CB}).

$\therefore \boldsymbol{\alpha} = \Delta I_C / \Delta I_E$ at V_{CB}= constant

The value of **α** in general is slightly lesser then unity.

Q.6. Explain why silicon transistor are preferably used. [Kanpur 2013,14]

Silicon is preferred over germanium due to few reasons that are mentioned as below

- At room temperature, silicon crystal has fewer free electrons than germanium crystal due to which silicon has smaller collector cut off current than germanium.
- The variation of collector cut off current with temp. is less in silicon compared to germanium.
- The structure of germanium crystals will be destroyed at higher temperature. However, Silicon crystals are not easily damaged by excess heat.
- Peak Inverse Voltage rating of silicon diodes is greater than germanium diodes.
- Silicon is less expensive due to its abundance.

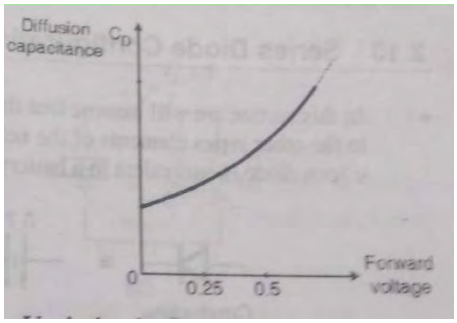
Q.7. Explain diffusion capacitance in transistor. [Kanpur 2016]

When the p-n junction diode is forward biased, a capacitance which is significant is known as **diffusion capacitance** (C_D) or storage capacitance.

- The diffusion capacitance (C_D) is given by ,

$$C_D = \frac{dQ}{dV} = \frac{dI(V)}{dV} T_F \quad , \quad \text{where } T_F = transist\ time$$

- The variation of diffusion capacitance with the change in forward voltage is shown in fig.
- In the forward biased state, C_D increases with the increase in forward bias .



Q.8. Draw the circuit diagram, explain the action of an n-p-n transistor in the common emitter configuration and obtain the expression for current gain given by β=α/(1-α). [Important]

Refer to Q.2 ,Q.3 & Q.9

Q.9. Draw the circuit diagram of a p-n-p transistor in the common bias configuration. Draw the characteristics curves and write its important features. [Important]

Refer to Q.2 & Q.3

Q.10. What do you mean by different current gains α, β &γ of a transistor ? Establish relation in them. [Kanpur 2014]

α is known as Current amplification factor in C-B Mode , defined as the ratio of the change in the collector current (ΔI_C) to the change in emitter current (ΔI_E) at a constant base- collector voltage (V_{CB}).

$\therefore \alpha = \Delta I_C / \Delta I_E$ at V_{CB}= constant

β is known as Current amplification factor in C-E Mode . It is the ratio of the change in the collector current (ΔI_C) to the change in base current (ΔI_B) at a constant collector-emitter voltage (V_{CE})

$\therefore \beta = \Delta I_C / \Delta I_B$ at V_{CE}= constant

γ is known as Current amplification factor in C-C Mode . It is the ratio of the change in the emitter current (ΔI_E) to the change in base current (ΔI_B) at a constant collector-emitter voltage (V_{CE})

$\therefore \gamma = \Delta I_E / \Delta I_B$ at V_{CE}= constant

Relation b/w α , β & γ

$\because I_E = I_B + I_C$

Dividing throughout by I_C , We have

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\Longrightarrow 1/\frac{I_E}{I_C} = 1/\frac{I_B}{I_C} + 1$$

$$\Longrightarrow 1/\alpha = 1/\beta + 1$$

$$\therefore \alpha = \beta / (\beta+1)$$

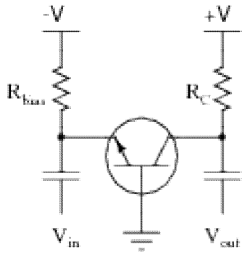
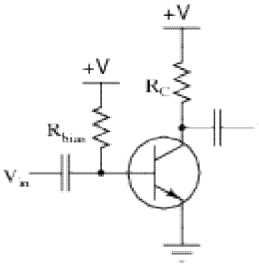
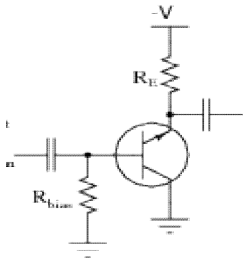
$$\therefore \beta = \alpha / (1-\alpha)$$

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_C + \Delta I_B}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} + 1 = \beta + 1$$

Also $\gamma = \alpha / (1-\alpha) + 1 = 1/(1-\alpha)$ $\{\because \beta = \alpha / (1-\alpha)\}$

Q.11. Compare the different characteristics of BJT configurations .

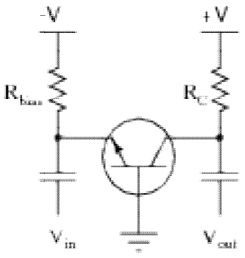
S. No.	Characteristics	CB Mode	CE Mode	CC Mode

1	Input resistance	Vary low≈100Ω	Low≈800Ω	Very High ≈800KΩ
2.	Output Resistance	Very High ≈550KΩ	High≈75Ω	Very low ≈50Ω
3	Current Gain	Less than 1	High 50 to 500	High ≈100
4.	Voltage gain	≈150	≈550	Less than 1
5.	Power gain	≈147	≈50,000	≈98
6.	Signal phase	As input	Opposite	Same as input
7.	Circuit			
8.	Application	In high frequency apparaatus	In audio frequency applications	In impedance matching

Q.12. Explain current gain & voltage gain of a transistor in different configurations .

[Kanpur 2016]

Common Base Configuration



Current Gain : It is the ratio of change in collector current to the change in emitter current, denoted by α , its value is near to unity. It is also defined as the ac current gain.

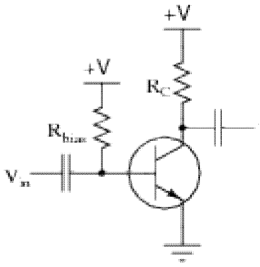
$$\alpha = \frac{\Delta i_c}{\Delta i_e}$$

Voltage Gain

It is the ratio of change in output voltage to change in input voltage, denoted by A.

$$A = \frac{\Delta V_{out}}{\Delta V_{input}} = \frac{\Delta i_c}{\Delta i_e}\frac{R_L}{R_i} = \alpha\frac{R_L}{R_i}$$

Common Emitter Configuration



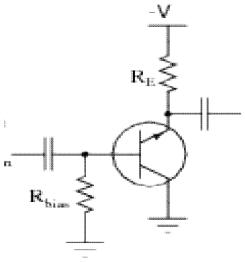
Current Gain: The ratio of change in collector current to the change in base current, denoted by β, $\beta = \frac{\Delta I_C}{\Delta I_B}$

Voltage gain

It is the ratio of change in output current to change in input current, denoted by A.

$$A = \frac{\Delta V_{out}}{\Delta V_{input}} = \frac{\Delta i_c}{\Delta i_B}\frac{R_L}{R_i} = \beta\frac{R_L}{R_i}$$

Common Collector Configuration



Current Gain: The ratio of change in emitter current to the change in base current, denoted by γ,

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Further $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{\frac{\Delta I_E}{\Delta I_C}}{\frac{\Delta I_E}{\Delta I_C} - 1} = \frac{\frac{1}{\alpha}}{\frac{1}{\alpha} - 1} = \frac{1}{1-\alpha} = \beta + 1$

Voltage gain

It is the ratio of change in output current to change in input current, denoted by A which value is lesser then unity.

Q.13. What do you mean by transistor load line ? How will you obtain a d.c. load line for a transistor ? What is its utility. [Important]

Or

Define load line & operating point.

The load line is defined as a line that contains every possible operating point for the circuit. To understand the concept of dc load line consider the common emitter configuration & the output circuit as shown in fig (a) & fig. (b) resp.

Procedure to obtain the DC load line :

- Refer to the collector circuit of the CE configuration & apply KVL to this circuit, we have $V_{CC} - V_{CE} - I_C R_C = 0$
- Rearranging the equation , We have
  $I_C = V_{CE}(-1/R_E) + V_{CC} / R_C$

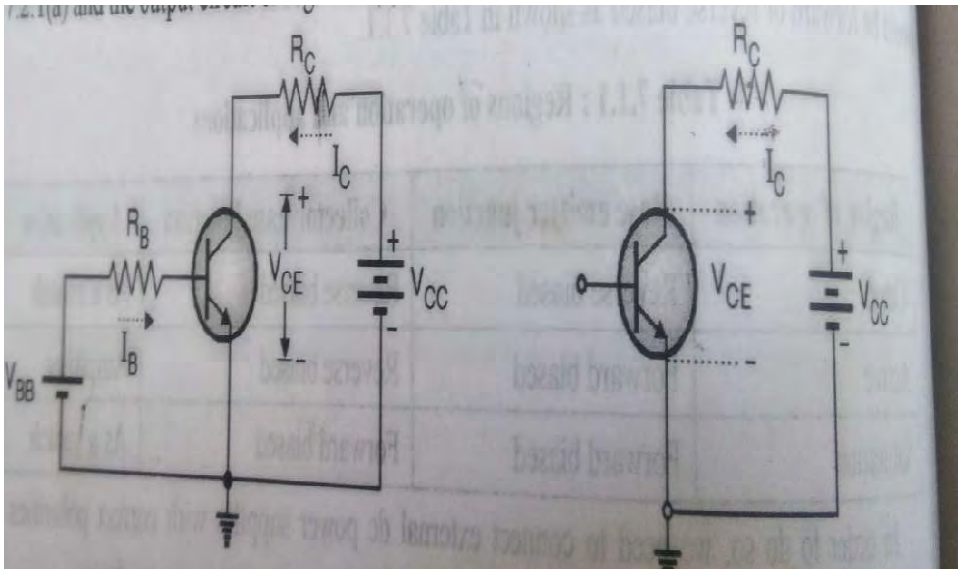


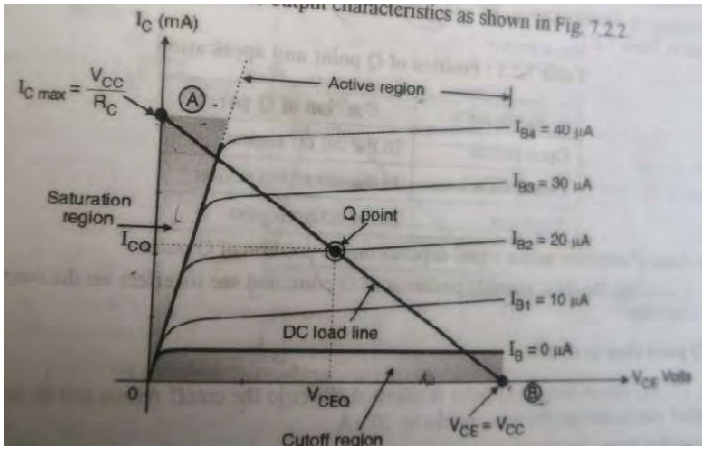
Fig. (a) Fig. (b)

- The above equation is the equation of a straight line ($y = mx + c$) with slope $-1/R_E$ & intercept V_{CC} / R_C.

- This straight line equivalency is known as dc load line.
- DC indicates that this line is drawn under dc operating conditions without ac signal at input

The Operating Point or Quiescent Point(Q-Point)

- It is a point on the load line which represents the dc current through a transistor (I_{CQ}) and the voltage across it (V_{CQ}), when no ac signal is applied. In short it represents the dc bias condition. The term Quiescent Point means quiet, still or inactive. The Q-point is also known as "Operating point" or "bias point".
- The position of operating point on load line is dependent on the application of the transistor. If the transistor is being used in for amplification purpose the Q-point should be exactly at the centre of load line
- Any point on the dc load line can be used as Q point.



Utility of transistor load line

- In absence of characteristics curve , the load line acts as a substitute , as it gives locus of all points of a curve where the device can be operated and a corresponding output can be obtained.

Q.14. Why common emitter amplifier is preferred to common bas amplifier ? [Important]

Or

Explain why the common emitter configuration is preferred for a transistor. [Important]

Out of the three configuration CE configuration is the most popular & widely used configuration , due to following reasons

- It has high voltage gain as well as high current gain
- As voltage gain as well as current gain is high , it has a very high power gain, as power gain is product of current gain & voltage gain.
- The CE configuration has moderate values of R_i & R_o, therefore many such stages can be coupled to each other without using any additional impedance matching circuits . Because of this property maximum power transfer takes place from one stage to other.
- Further ref. to Q. 11.

Q.15. Explain the term base width modulation in transistor. [Kanpur 2016]

The modulation of effective base width due to collector voltage (V_{CC}) is known as **width modulation** or **Early effect.**

As the collector to emitter voltage V_{CC} is made to increase the reverse bias , the space charge width between collector and base tends to increase, with the result that the effective width or the base decreases. This dependency of base width on collector to emitter voltage is known as the base width modulation or early effect.

- Recombination chances decreased within the base region. Hence α(common base current amplification) increases with increasing V_{CC} . β also increases for CE configuration.
- The current of minority carriers injected across the emitter junction increases.
- Very large reverse bias may cause voltage breakdown in the transistor. This is due to reduction of effective base width to zero.

Q.16. Define & discuss base spreading resistance

Base is lightly doped thin region, that becomes thinner due to spread of the two depletion regions . It offers a resistance to the passing currents, that is known as base spreading resistance. The value of this base spreading resistance r_v is of the order of hundred volts.

- Base spreading resistance is contributed by three factors i.e. the base is narrow, it is a very thin slice and doping is low .
- Base Emitter Resistance is a resistance that provides the required amount of automatic biasing needed for a common emitter amplifier

Q.17. Explain transit time for minority carriers. Derive an expression for it.[Kanpur 2014,16]

There are two dominant features of p-n junctions, the injection of minority carrier with forward bias & the variation of depletion width W with reverse bias.

- To have a good p-n-p transistor , we prefer that almost all holes injected by the emitter into the base be collected.
- Thus n-type base region should be narrow & the hole life time t_p should be long i.e. $W_b << L_p$, where W_b is the length of the neutral n-type material & L_p is the diffusion length.
- There is an important difference in the times which electrons & holes spend in the base. The average excess hole spends a time $\tau_{p,}$ defined as the **transit time from emitter to collector.**
- Since the base width W_b is made smaller then length L_p , the transit time is much less than the average hole life time τ_p in the base.
- On the other hand an average excess electron supplied from the base contact spend τ_p second in the base supplying space charge neutrality during the life time of an average excess hole.
- While the average electron waits τ_p seconds for recombination , many individual holes can enter and leave the base region , each with an average transit time τ_t .
- The ratio of τ_p & τ_t is β i.e. $\beta = {}^{\tau_p}/_{\tau_t} = {}^{i_c}/_{i_b}$

Calculation of transit time: Consider that the diffusing holes seem to have an average velocity $v(x_n)$.

The transit time is

$$\tau_t = \int_0^{w_b} \frac{dx_n}{v(x_n)} = \int_0^{w_b} \frac{qAp(x_n)}{i_p(x_n)} dx_n$$

For the triangular distribution, the diffusion current is almost constant at

$i_p = qAD_p \frac{\Delta p_E}{w_b}$ & τ_t becomes

$$\tau_t = \frac{qA\Delta p_E {}^{w_b}/_2}{qAD_p\Delta p_E / w_b} = \frac{w_b^2}{2D_p}$$

Q.16. Explain Life time of minority carrier .

Carrier lifetime is defined as the average time it takes for a minority carrier to recombine. The process through which this is done is typically known as minority carrier recombination.

- Carrier lifetime plays an important role in bipolar transistors and solar cells.
- In indirect band gap semiconductors, the carrier lifetime strongly depends on the concentration of recombination centers.
- Gold atoms act as highly efficient recombination centers
- Silicon for some high switching speed diodes and transistors is therefore alloyed with a small amount of gold. Many other atoms, e.g. iron or nickel, have similar effect.

Numerical

Q.1. Current amplification factor of a common base configuration is 0.88. Find the value of base current when the emitter current is 1mA. [Important]

Exp: Given Current amplification factor (α) = 0.88, I_E= 1mA

For CB configuration $\alpha = I_C / I_E$

$\because I_E = I_B + I_C$

$\therefore I_E = I_B + \alpha I_E$

$\Rightarrow I_B = I_E * (1 - \alpha)$

$= 1mA * (1-0.88) = 0.12mA$ Ans

Q.2. The constant α of a transistor is 0.95. What would be the change in the collector current corresponding to a change of 0.4mA in the base current in the common emitter configuration.

[Important]

Exp: Given α= 0.95, ΔI_B= 0.4mA, ΔI_C= ?

$\because \beta = \alpha / (1 - \alpha)$

$\therefore \beta = 0.95/(1-0.95) = 19$

Also $\beta = \Delta I_C / \Delta I_B \Rightarrow \Delta I_C = \beta * \Delta I_B$

$\therefore \Delta I_C = 19 * 0.4mA = 7.6$ mA Ans

Q.3. The load resistance of the output circuit in a common emitter amplifier is 400 kΩ and the input resistance is 300Ω. If current gain is common base configuration is 0.95, then find the voltage amplification. [Important]

Exp: Given Load resistance(R_L)= 400kΩ, Input resistance(R_{in})= 300Ω, α= 0.95

$\because \beta = \alpha / (1 - \alpha) \Rightarrow \beta = 0.95/(1-0.95) = 19$

$\because$ Voltage amplification = Voltage gain

and Voltage gain = Output voltage/ Input voltage

For CE configuration output voltage= $\Delta I_C R_L$

Input Voltage= $\Delta I_B R_{in}$

$\therefore$ Voltage gain = $\Delta I_C R_L / \Delta I_B R_{in} = (\Delta I_C / \Delta I_B) * (R_L / R_{in}) = \beta * (R_L / R_{in})$

$= 19 * (400\ k\Omega / \mathbf{300\Omega}) = 25.33 \times 10^3$ Ans

Q.4. In the CE configuration, the voltage drop across a resistance of 6kΩ connected in the collector circuit is 6volts. If the current gain in the CB configuration of the transistor is 0.995, then find the base current I_b. [Important]

Exp: Given $R_L = 6k\Omega$, $V_0 = 6V$, $\alpha = 0.995$

$\because \beta = \alpha /(1- \alpha) \Rightarrow \beta = 0.995/(1-0.995) = 199$

Also $\beta = I_C/I_B = (V_0/R_L)/ I_B$

$\Rightarrow 199 = (6V/6k\Omega)/ I_B$

$\Rightarrow I_B = (6V/6k\Omega)/199 = 5.025\mu A$ Ans

Q.5. The reverse Saturation current in a an NPN transistor in CB configuration is 12.5μA. For an emitter current of 2mA, the collector current is 1.97mA. Determine current gain & base current. [Important]

Exp: Given ,Reverse Saturation current (I_{CBO})= 12.5×10^{-3}mA, I_E=2mA , I_C= 1.97mA , I_B= ?,

α= ?

We know that $I_C = \alpha I_E + I_{CBO}$

$\therefore \alpha = (I_C - I_{CBO})/ I_E$

$\alpha = (1.97mA - 12.5 \times 10^{-3}mA)/ 2mA = 0.978$ Ans

Also $I_E = I_B + I_C \Rightarrow I_B = I_E - I_C$

$\therefore I_B = 2mA - 1.97mA = 0.03mA$

Q.6. In a transistor circuit when the base current is increased by 50μA keeping collector voltage fixed at 2 volts, the collector current increases by 1mA. Calculate the current amplification factor α and β of the transistor. [Important]

Exp: Given $\Delta I_B = 50\mu A$, $V_C = 2Volt$, $\Delta I_C = 1mA$, α and β =?

$\because \beta = \Delta I_C/ \Delta I_B \Rightarrow \beta = 1mA/ 50\mu A = 10^{-3}/ 50 * 10^{-6} = 20$ Ans

$\because \alpha = \beta/ (\beta+1)$

$\therefore \alpha = 20/21 = 0.952$ Ans

Q.7. A silicon NPN transistor (β=100) I_{CO}= 22nA is operated in CE configuration as shown in fig. Determine the collector current if the transistor is in active region, V_{BE}=0.7v. Here V_{BB}= 5V , R_S= 220kΩ , R_L= 3.3kΩ & V_{CC}= 12V. [Important]

Exp: Given I_{CO}= 22nA , β=100, V_{BE}=0.7v,

V_{BB}= 5V , R_S= 220kΩ , R_L= 3.3kΩ & V_{CC}= 12V

I_C =?

Applying KVL to input side of CE configuration given

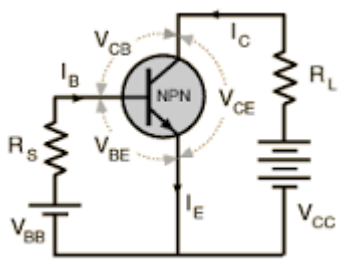
We have $-V_{BB} + I_B R_S + 0.7 = 0$

$I_B = (V_{BB} - 0.7) / R_S$

$I_B = (5-0.7) / 220k\Omega = 1.95 \times 10^{-5}A$

$\because I_C = \beta I_B + (1+ \beta) I_{CO}$

$\therefore I_C = 100 * 1.95 \times 10^{-5} + (1+100) 22 \times 10^{-9}$



$= 195x\ 10^{-5} + 101x22x\ 10^{-9}$

$= 195.22 \times 10^{-5}$ A Ans

Q.8. In a CB configuration , current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current. [Kanpur 2013]

Exp: Given $\alpha = 0.9$, $I_E = 1mA$, $I_B = ?$

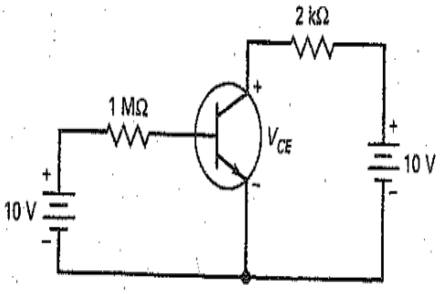
$\because \alpha = I_C / I_E$

$\therefore I_C = \alpha * I_E = 0.9x\ 1mA = 0.9mA$

$\because I_E = I_B + I_C$

$\therefore I_B = I_E - I_C \Rightarrow I_B = 1mA - 0.9mA = 0.1mA$ Ans

Q.9. The transistor of fig. has $\beta_{dc}=300$, Calculate I_B, I_C, V_{CE} and P_D.



Exp: Given $\beta_{dc}=300$,

For base current , I_B

Applying KVL at the input side we have

$-10V + 1M\Omega \cdot I_B + 0.7 = 0$

$\Rightarrow$ $I_B = (10-0.7) / 10^6 = 9.3\mu A$

For collector current

$\because I_C = \beta_{dc} I_B$

$\therefore I_C = 300x9.3\mu A = 2.79mA$

For Collector- emitter voltage

Applying KVL at the output side we have

$-10 + 2k\Omega . I_C + V_{CE} = 0$

$V_{CE} = 10 - 2x\ 10^3 \times 2.79 \times 10^{-3}$

$= 4.42$ V

For Collector power dissipation i.e. P_D

$P_D = V_{CE} I_C = (4.42V)(2.79mA) = 12.3$ mW Ans

Q.10. What are the saturation current and the cutoff voltage in fig.

Exp: During Saturation $V_{CE}=0$ V

$\therefore$ Applying KVL at the output side, we have

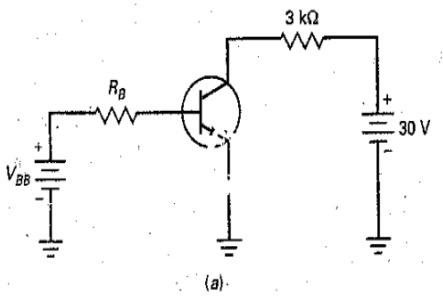
$-30 + 3K\Omega . I_C - V_{CE} = 0$

$\Rightarrow$ $-30 + 3K\Omega . I_C - 0 = 0$ $\{\because\}$

$\therefore I_C = 30/(3 \times 10^3) = 10mA$

During Cutoff Collector to emitter terminal is open

$\therefore V_{CE} = 30V$ Ans



Chapter-4
Transistor Biasing and Stabilization

Biasing

We known that transistor can operate i**n a**ny of three regions of operation namely cutoff, active region and saturation. To operate the transistor in these regions the two junction of a transistor should be forward or reversed biased as shown in table

Region of operation	Base Emitter Junction	Collector base junction	Application
Cut off	Reversed bias	Reversed bias	As a switch
Active	Forward bias	Reversed bias	Amplifier
Saturation	Forward bias	Forward bias	As a switch

In order to do so, we need to connect external DC power supplies with correct polarities & magnitude. This process is called as biasing of transistor.

Voltage divider bias (VDB)

The most famous circuit based on the emitter-bias prototype is called voltage divider bias. You can recognize it by the voltage divider in the base circuit.

Accurate VDB Analysis

The Key idea is for the base current to be much smaller than the current through the voltage divider. When the condition is satisfied, the voltage divider holds the base voltage almost constant and equal to the unloaded voltage out of the voltage divider. This Produces a solid Q point under all operating conditions

VDB load line & Q point

The load line is drawn through saturation and cut off. The Q point lies on the load line with the exact location determined by the biasing. Large variations in current gain have almost no effect on the Q point because this type of bias sets up a constant value of emitter current.

Two –Supply emitter bias

This design uses two power supplies: one positive and the other negative . The idea to set up a constant value of 'emitter current'.

Other types of bias

This section introduced negative feedback, a phenomenon that exits when an increase in an output quantity , produces decreases in an input quantity. It is brillent idea that led to voltage-divider bias. The other type of bias cannot use enough –ve feedback, so they fail to attain the performance level to voltage-divider bias.

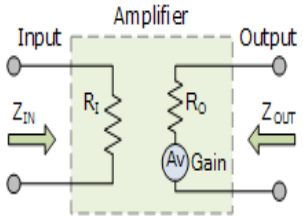
PNP Transistors

These pnp devices have all current & voltages reversed from their npn counterparts. They may be used with negative power supplies; more commonly, they are used with +ve power supplies in an upside-down configuration.

Reverse Feedback ratio

If some percentage of an amplifier's output signal is connected to the input, so that the amplifier amplifies part of its own output signal, we have what is known as feedback. Feedback comes in two varieties: positive (also called regenerative), and negative (also called degenerative). Positive feedback reinforces the direction of an amplifier's output voltage change, while negative feedback does just the opposite.

Input & Output impedances



It is the input impedance "seen" by the source driving the input of the amplifier. $\mathbf{Z_{in}}$ or Input Resistance is an important parameter in the design of a transistor amplifier and as such allows amplifiers to be characterized according to their effective input and output impedances as well as their power and current ratings.

For details refer to chapter 3

Bias Stabilization

The stability of a system is a measure of the sensitivity of a network to variations in its parameter. B increases with increase in temperature . Magnitude of V_{BE} decreases about 7.5 mV per degree Celsius (°C) increase in temperature. I_{CO}(reverse saturation current): doubles in value for every 10°C increase in Temperature

Stability Factors, S(I_{CO}), S(V_{BE}), and S(β)

A stability factor,S, is defined for each of the parameters affecting bias stability as listed below:

$$S(I_{CO}) = \Delta I_C / \Delta I_{CO}$$
$$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$$
$$S(\beta) = \Delta I_C / \Delta \beta$$

In each case, the delta symbol signifies change in that quantity.

BJT Transistor modeling

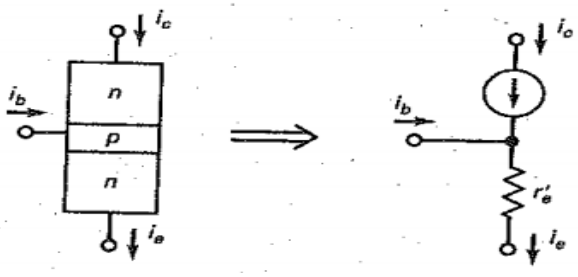
A model is the combination of circuit elements , properly chosen, the best approximates the actual behavior of a semiconductor device under specific operating conditions.

The ac equivalent of a network is

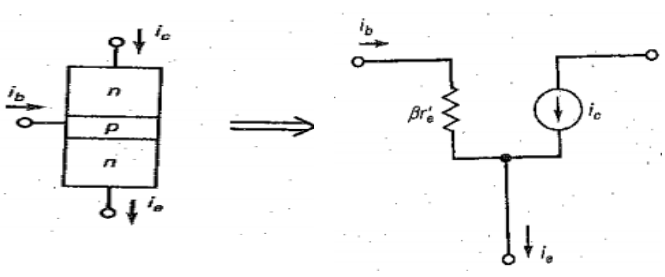
1. Setting all dc sources to zero and replacing them by a short- circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent.
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 & 2.
4. Redrawing the network in a more convenient and logical form.

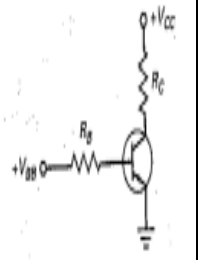
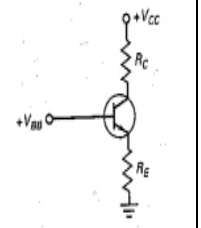
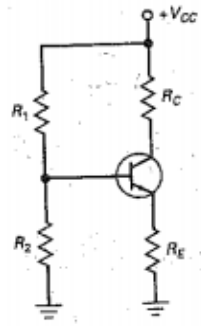
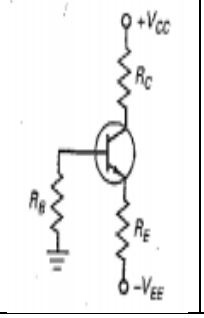
Transistor Model

The T- Model (Ebers- Moll model)



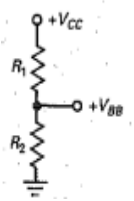
The π Model



Type	Circuit	Calculations	Characteristics	Where used
Base bias		$I_B= (V_{BB}-0.7V)/R_B$ $I_C=\beta I_B$ $V_{CE}= V_{CC} - I_C R_C$	Few parts; β dependent; fixed base current	Switch; digital
Emitter bias		$V_E=V_{BB} -0.7V$ $I_E= V_E/ R_E$ $V_C= V_C-I_C R_C$ $V_{CE}=V_C-V_E$	Fixed emitter current; β independent	I_C driver ; amplifier
Voltage divider bias		$V_B=$ $R_2V_{CC}/(R_1+ R_2)$ $V_E= V_B-0.7V$ $I_E= V_E/ R_E$ $V_C= V_{CC}-I_C R_C$ $V_{CE}= V_C - V_E$	Needs more resistors; β independent; needs only one power supply	Amplifier
Two – supply emitter bias		$V_B = 0V$ $V_E= V_B-0.7V$ $V_{RE}=V_{EE}-0.7V$ $I_E=V_{RE}/R_E$ $V_C= V_{CC}- I_C R_C$ $V_{CE}= V_C- V_E$	Needs positive & negative power supplies; β independent;	Amplifier

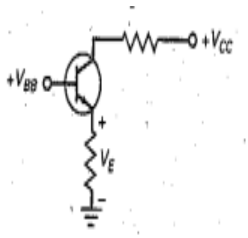
VDB Derivations

Base voltage



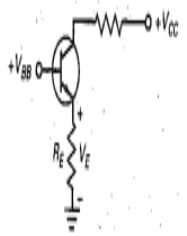
$V_{BB}= R_2V_{CC}/(R_1+ R_2)$

Emitter voltage



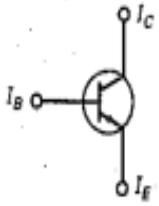
$V_E= V_{BB}- V_{BE}$

Emitter current



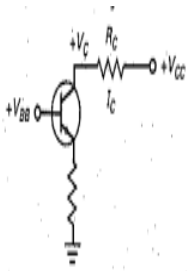
$I_E = V_E / R_E$

Collector current



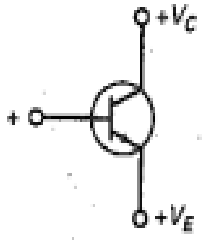
$I_C \approx I_E$

Collector voltage



$V_C = V_{CC} - I_C R_C$

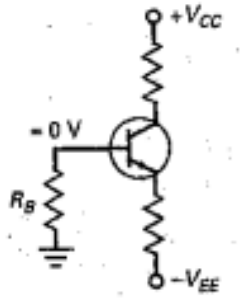
Collector – emitter voltage



$V_{CE} = V_C - V_E$

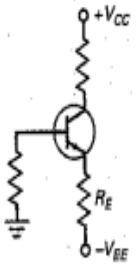
TSEB (Two supply emitter bias) Derivations

Base voltage



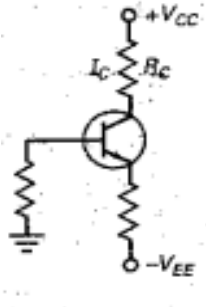
$V_B \approx 0$

Emitter current



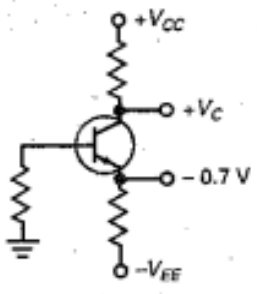
$V_C = V_{CC} - I_C R_C$

Collector Voltage (TSEB)



$V_C = V_{CC} - I_C R_C$

Collector-emitter Voltage (TSEB)



$V_{CE} = V_C + 0.7V$

Long & Short Questions

Q.1. What is meant by transistor –biasing ? Define Stability factor. [Kanpur 2015]

Or

What do you understand by transistor by transistor biasing ? Why it is necessary ?

Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

Necessary of transistor biasing

- To active an transistor, biasing is essential. For proper working it is essential to apply to apply voltages of correct polarity across its two junctions.
- If it is not biased correctly it would work inefficiently and produce distortion in the output signal
- Q-point is not middle Output signal is distorted & the signal is clipped
- Further for various applications , BJT is biased as shown in table

Region of operation	Base Emitter Junction	Collector base junction	Application
Cut off	Reversed bias	Reversed bias	As a switch
Active	Forward bias	Reversed bias	Amplifier
Saturation	Forward bias	Forward bias	As a switch

- In order to have these applications , we need to connect external DC power supplies with correct polarities & magnitude. This process is called as biasing of transistor.

Stability Factor

The stability of Q point of transistor amplifier depends on the following three parameters :

1. Leakage current I_{CO} 2. β_{dc} 3. Base to emitter voltage

The effect of these parameters can be expressed mathematically by defining the stability factors

1. Stability factor $S = \frac{\Delta I_C}{\Delta I_{CO}} \Big|$ Constant V_{BE} & β_{dc}

   This represents the change in collector current due to change in reverse saturation current I_{CO} The other two parameters that means V_{BE} & β_{dc} are assumed to be constant.

2. Stability factor $S' = \frac{\Delta I_C}{\Delta V_{BE}} \Big|$ Constant I_{CO} & β_{dc}

S' represents the change in I_C due to change in V_{BE} at constant I_{CO} & β_{dc}

3. Stability factor $S'' = \left.\frac{\Delta I_C}{\beta dc}\right|_{\text{Constant } I_{CO} \& V_{BE}}$

Total change in collector current

$\Delta I_C = S.\Delta I_{CO} + S'.\Delta V_{BE} + S''.\beta dc$

- Ideally the values of all the stability factors should be zero and practically they should be as small as possible.
- Practically the value of S is significantly higher than the other two stability factor. Hence while comparing the biasing circuits, the values of S is more significant.

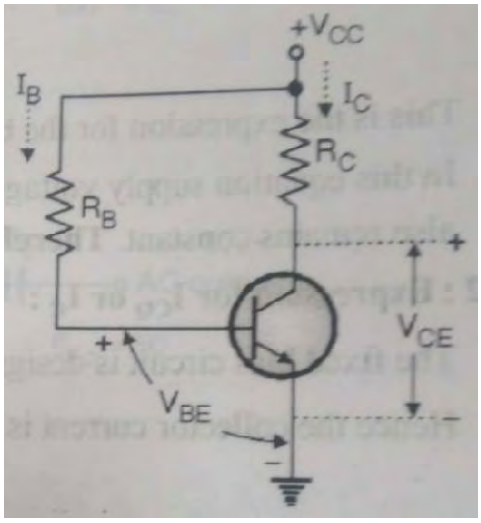
Q.2. What are the various methods used for transistor biasing? Explain one method & State its advantage & disadvantages.

Related Short Answer Questions

(i) What do you mean by biasing of a transistor ? Explain with examples [Kanpur 2014]

Biasing is a technique to aid V_{BB} in the input circuit which is separate from the V_{CC} used in the output circuit. The following are the most commonly used method for transistor biasing are as below :

1. Fixed bias circuit (Single base resistor biasing) or base bias
2. Collector to base bias circuit
3. Voltage divider bias circuit (VDB) or self bias
4. Emitter bias or modified fixed bias circuit



Fixed bias circuit (Single base resistor biasing) or base bias

The simplest of all biasing is fixed bias ckt. as shown in fig.

- Before biasing we were using two separate power supplies i.e. V_{CC} & V_{BB} to bias a transistor.
- But in this circuit only one power supply has been used to supply power to both collector as well as base.
- R_B is the single base biasing resistor , hence this circuit is also called as single base resistor biasing.

Analysis of Fixed bias circuit :

As shown in fig. splitting input & output terminals in two loops , namely base circuit & collector circuit

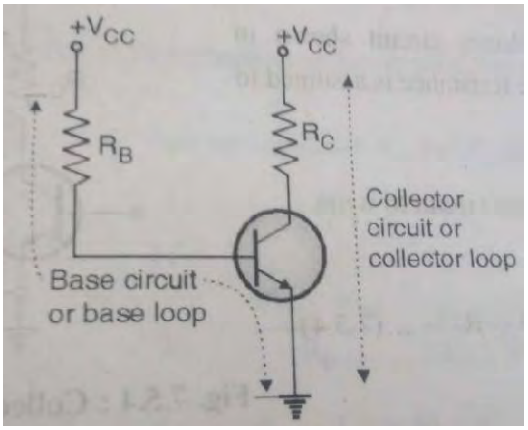


Fig. (a)

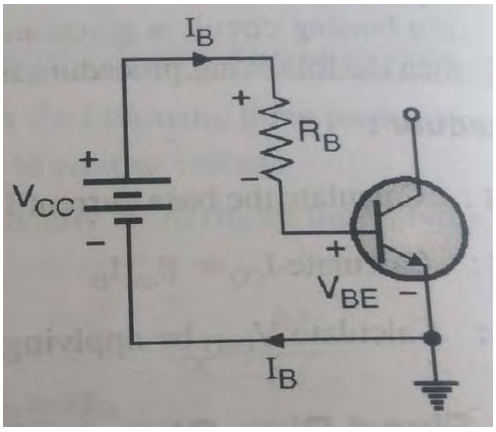


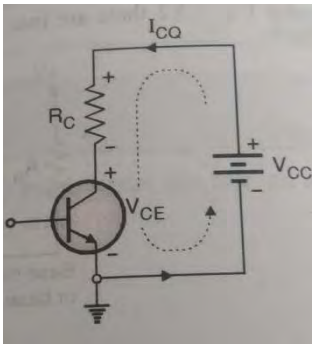
Fig. (b)

as shown in fig.(a).

Expression for I_B

- Consider the base circuit as shown in fig.(b) . Applying KVL to the base circuit we have
  $- V_{CC} + I_B R_B + V_{BE} = 0$
- Rearranging the equation we get
  $I_B = (V_{CC} - V_{BE})/ R_B$
- For silicon V_{BE}= 0.7 and for germanium V_{BE}= 0.3V

Expression for I_C & V_{CE}



Since the fixed bias is operated in the active region therefore

$I_C = \beta I_B + I_{CEO}$

$\because \beta I_B >>> I_{CEO}$

$\therefore I_C = \beta I_B$

Applying KVL to the collector circuit shown , we have

$V_{CC} - I_C R_C - V_{CE} = 0$

$\therefore \quad V_{CE} = V_{CC} - I_C R_C$

Advantages

1. The fixed bias circuit is simple and less number of components.
2. It give very good flexibility as the Q point can be set at any point in the active region by just adjusting the value of R_B .

Disadvantages

1. Vary poor thermal stability as S= 1 + β_{dc}.
2. With changes in β_{dc} due to change in temp. , the operating point keeps on shifting its position.

Q.3. What do you understand by 'Bias stability' of a transistor ? Why is it necessary ? Explain the working of self-bias circuit for common emitter BJT. [Kanpur 2015]

Or

Draw the circuit diagram of voltage diagram of voltage divider bias of a transistor . Explain its working. [Important]

For definition ref. Q.1

Self Bias

The voltage –divider biasing is known as self bias circuit. The circuit for voltage- divider bias is shown in fig. (a) . The resistance R_1 & R_2 form a potential divider to apply a fixed voltage V_B to the base.

A resistance R_E has been connected in the emitter circuit. This resistance is not present in the fixed bias or collector to base bias circuits.

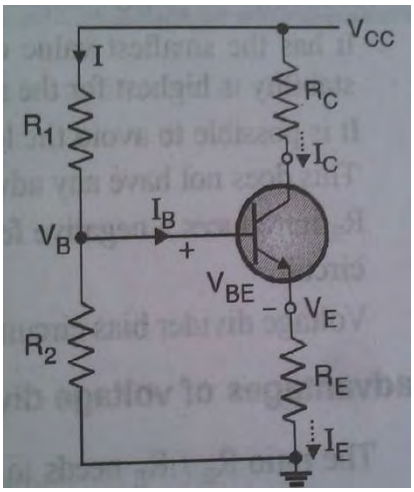


Fig. (a)

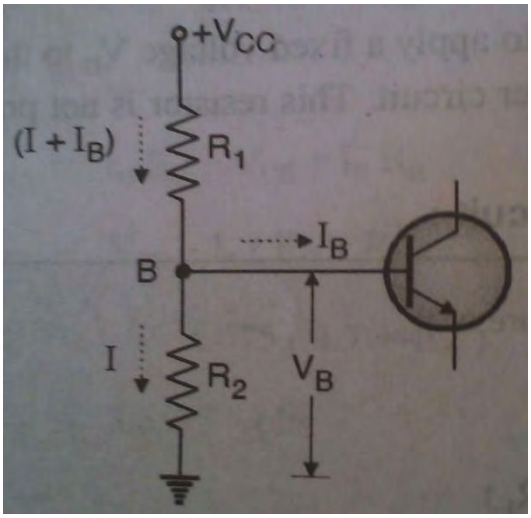


Fig. (b)

Analysis of Voltage divider bias circuit

Base circuit

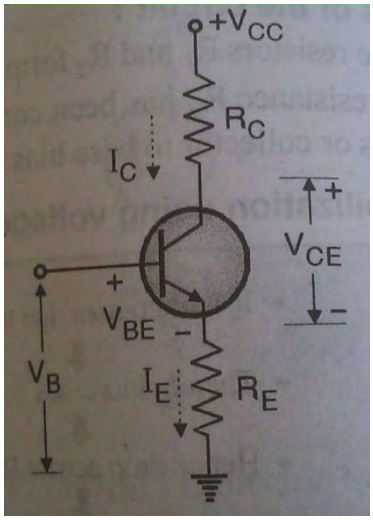
The base circuit as shown in fig(b) . Here we have considered collector & emitter terminals as open circuited . The base Voltage V_B is nothing but the voltage across resistor R_2

i.e. $V_B = \frac{R_2}{R_1+R_2} V_{CC}$

This is because , current through R_1 & R_2 is approx. same and is equal to I.

Collector circuit

The collector circuit as shown in fig., the voltage across emitter resistance R_E can be as follows :



$$V_E = I_E R_E = V_B - V_{BE}$$

$$\therefore \quad I_E = (V_B - V_{BE}) / R_E$$

Applying the KVL to the collector circuit we get

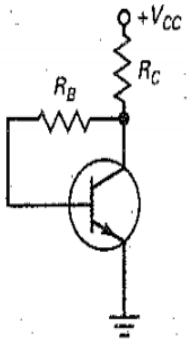
$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$
$$\therefore V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$V_{CE} = V_{CE} - I_E R_E - I_C R_C$$

Bias stabilization

- If I_C increases due to change in temp. or β
- Then I_E increases
- Hence drop across R_E increases ($V_E = I_E R_E$)
- But V_B is constant. Hence V_{BE} decreases.
- Hence I_B decreases.
- Hence I_C also deceases. Thus the compensation for increase in I_C is achived.

Q.4. Draw the circuit diagram of Collector to base bias of a transistor . Explain its working.

Collector to base bias shown in fig. is also known as collector-feedback bias. Historically , this was another attempt at stabilizing the Q point. Again, the basic idea is to feed back a voltage to the base in an attempt to neutralized any change in collector current.



Like emitter-feedback bias circuit , collector feedback bias circuit uses –ve feedback in an attempt to reduce the original change in collector current.

Analysis

Applying KVL in the base circuit we have

$$-V_{CC} + R_C(I_C + I_B) + I_B R_B + V_{BE} = 0$$

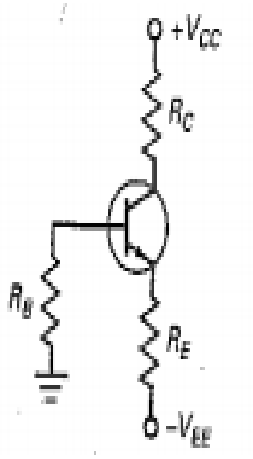
$\because I_B = I_C/\beta$

$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta}$

Similarly applying KVL on collector side

We have $V_C = V_{CE} = V_{CC} - I_C R_C$

Q.5. Draw the circuit diagram of two supply emitter bias of a transistor . Explain its working.



Sometimes electronic equipment has a power supply that produces both +ve and –ve supply voltages. The –ve supply forward biases the emitter diode. The +ve supply reverse bias the collector diode.

This circuit is derived from emitter bias, for this reason , we refer to it as two-supply emitter bias (TSEB).

Analysis

$V_B \approx 0$ V

Applying KVL from emitter to base loop in anticlockwise we have

$V_{EE} - I_E R_E - V_{BE} = 0$

$\therefore - I_E = (- V_{EE} + V_{BE}) / R_E = (-V_{EE} + 0.7) / R_E$

$\therefore I_E = (V_{EE} - 0.7) / R_E$

$V(R_E) = V_{EE} - 0.7$ V

Applying KVL on collector side we have

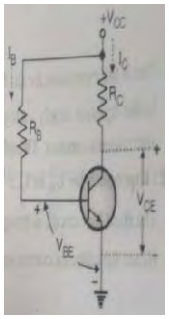
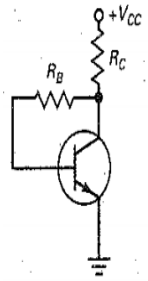
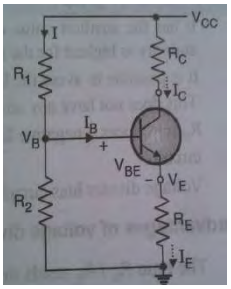
- $V_{CC} + I_C R_C + V_C = 0$

$\therefore V_C = V_{CC} - I_C R_C$

$V_{CE} = V_C - V_E$

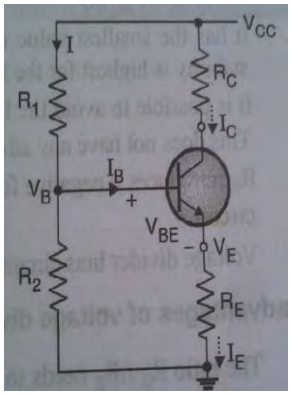
Q.7. Compare Fixed bias, Collector to base bias & Voltage divider bias circuits.

Sr. No.	Parameter	Fixed bias	Collector to base bias	Voltage divider bias
1.	Emitter Resistance	Not used	Not used	Used
2.	-ve Feedback	Not used	Included	Included
3.	Stability	S= (1+ β)	S = (1+ β)/ [1+	S=(1+ β) * [1+ $\frac{R_B}{R_C}$] /

	factor		$\beta(\frac{R_C}{R_{C+}R_B})]$	$[1+\beta+\frac{R_B}{R_C}]$
4.	Q-Point stability	Poor	Moderate	Good
5.	Configuration			

Numerical

Q.1. **Determine I_C, V_E, V_B& V_C for the voltage divider configuration .If β=20, R_1= 62KΩ, R_2= 9.1 KΩ , R_C= 3.9 KΩ ,R_E= 0.68 KΩ &V_{CC}= 16V**



Exp: As the biasing is voltage divider

We have $V_B = V_{CC}. R_2/ (R_1+R_2)$

$\therefore V_B = 16 \times \frac{9.1k\Omega}{62k\Omega+9.1k\Omega} = 2V$

$\because V_E = V_B - V_{BE}$

$\therefore V_E = 2V - 0.7V = 1.3V$

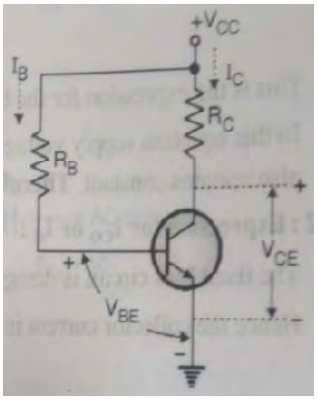
$\because I_E = V_E / R_E$

$\therefore I_E = 1.3V / 0.68K\Omega = 1.23mA$

$\because I_C = \alpha . I_E = \beta /(\beta+1) I_E$

$\therefore I_C = 1.23mA \times 20/21 = 1.17mA$

Q.2. **For the fixed bias circuit determine I_B, I_C, V_{CE}, V_B, V_C&V_{BC} for the following parameters R_B = 240 KΩ , R_C= 2.2 KΩ , V_{CC}= 12 V & β=50**



Exp: As it is fixed bias

We have $I_B = (V_{CC} - V_{BE})/ R_B$

$\therefore I_B = (12-0.7)/ 240\ K\Omega$

$= 47.08\mu A$

$\because I_C = \beta I_B$

$\therefore I_C = 50 \times 47.08\mu A = 2.35mA$

$\because V_{CE} = V_{CC} - I_C R_C$

$\therefore V_{CE} = 12 - 2.35mA \times 2.2\ K\Omega$

$= 6.83\ V$

$\because$ Emitter terminal is grounded

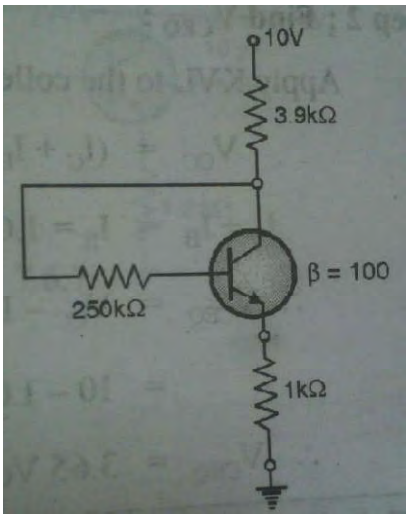
$\therefore V_B = V_{BE} = 0.7V$

$V_C = V_{CE} = 6.83\ V$

$\because V_{BC} = V_B - V_C$

$\therefore V_{BC} = 0.7V - 6.83V = 6.13\ V$

Q.3. Determine the values of I_C & V_{CE} for the biasing circuit shown in fig.



Exp: As per the given parameters in Collector-emitter feedback

Applying KVL on input side, we have

$-10 + 3.9k\Omega(I_C + I_B) + 250k\Omega.\ I_B + V_{BE} + 1\ k\Omega.\ I_E = 0$

$\because I_E = (1+\beta)I_B\ ,\ I_C = \beta I_B\ ,V_{BE}=0.7$ and $\beta = 100$

$\therefore\ -10 + 3.9k\Omega(\beta I_B + I_B) + 250k\Omega.\ I_B + 0.7 + 1\ k\Omega.\ (1+\beta)I_B = 0$

$I_B = 9.3/\ [3.9k\Omega(1+\beta) + 250k\Omega + 1\ k\Omega\ (1+\beta)]$

$I_B = 9.3/\ [3.9k\Omega(1+100) + 250k\Omega + 1\ k\Omega\ (1+100)]$

$I_B = 12.48\ \mu A$ Ans

Q.4. Determine the voltage gain of a single stage CE transistor if the effective resistance of collector circuit is 2kΩ , input resistance is 1kΩ & current gain is 50. [Important]

Exp: Given $R_C = 2k\Omega$, $R_{in} = 1k\Omega$ & $\beta = A_i = 50$

$\because A_V = \beta\frac{R_L}{R_{in}}$

$\therefore A_V = 50 * \frac{2k\Omega}{1k\Omega} = 100$ Ans

Q.5. Determine V_C and V_B for the network of Fig.

Exp: Applying KVL in the anticlockwise for the base-emitter loop , we have

$+V_{EE} - V_{BE} - I_B R_B = 0$

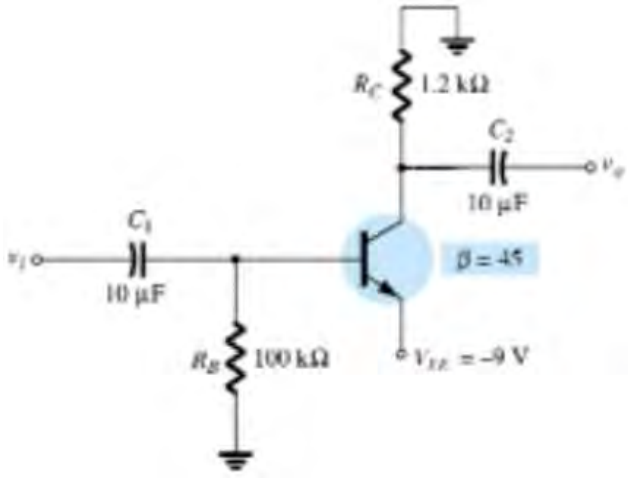
$\therefore I_B = (V_{EE} - V_{BE})/\ R_B$

$\therefore I_B = (9-0.7)/\ 100\ k\Omega = 83\mu A$

$\because I_C = \beta\ I_B$

$\therefore I_C = 45 \times 83\mu A = 3.735\ mA$

$\because V_C = -\ I_C\ R_C$



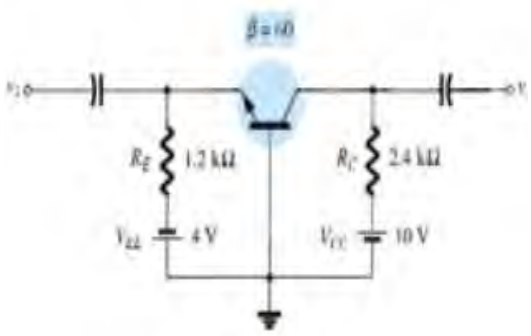
$\therefore V_C = -\ 3.735\ mA \times 1.2\ k\Omega = -4.48\ V$

$\because V_B = -\ I_B\ R_B$

$\therefore V_C = -83mA \times 100\ k\Omega = -8.3\ V$

Q.6. Determine the voltage V_{CB} and the current I_B for the common-base configuration for the given fig.

Exp: Applying KVL to the input circuit yields



$-V_{EE} + I_E R_E + V_{BE} = 0$

$\therefore I_E = (V_{EE} - V_{BE}) / R_E = (4-0.7)/ 1.2k\ \Omega = 2.75mA$

Applying KVL to the output circuit yields

$-V_{CC} + I_C R_C + V_{CB} = 0$

$\therefore V_{CB} = V_{CC} - I_C R_C$

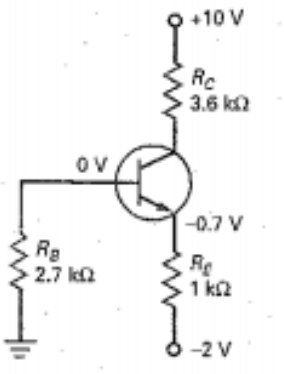
$\because I_C \approx I_E$

$\therefore V_{CB} = 10 - 2.75mA \times 24\ k\ \Omega = 3.4V$

$\because I_B = I_C / \beta$

$\therefore I_B = 2.75mA / 60 = 45.8\mu A$ Ans

Q.7. What is the collector voltage in the given circuit



Exp: Applying KVL at the Emitter base terminal we have

$+ 2V - 1k\ \Omega \times I_E - V_{BE} = 0$

$\therefore I_E = (\ 2 - 0.7\ ) / 1k\ \Omega = 1.3mA$

$\because V_C = V_{CC} - I_C R_C$

Also $I_C \approx I_E$

$\therefore V_C = 10 - 1.3mA \times 3.6k\ \Omega$

5.32 V Ans

Chapter-5
Two port networks

A two-port network is a four- terminal circuit in which the terminals are paired to form an input port and an output port. Different models for two port networks are

Model Name	Express	In terms of	Defining equations
Impedance	V_1, V_2	I_1, I_2	$V_1 = z_{11}I_1 + z_{12}I_2$ and $V_2 = z_{21}I_1 + z_{22}I_2$
Admittance	I_1, V_2	V_1, V_2	$I_1 = y_{11}V_1 + y_{12}V_2$ and $I_2 = y_{21}V_1 + y_{22}V_2$
Hybrid	V_1, I_2	I_1, V_2	$V_1 = h_{11}I_1 + h_{12}V_2$ and $I_2 = h_{21}I_1 + h_{22}V_2$
Transmission	V_1, I_1	$V_2, -I_2$	$V_1 = AV_2 - BI_2$ and $I_1 = CV_2 - DI_2$

Hybrid Parameters

Every linear circuit having input and output terminals can be analyzed by four parameters (one measured in ohm, one in mho and two dimensionless) called hybrid or h Parameters. Hybrid means "mixed". Since these parameters have mixed dimensions, they are called hybrid parameters. Transistor is a three terminal device but for practical purpose it need four terminals two used for input & two for output.

Nomenclature for Transistor h Parameters

S. No.	h parameter	Notation in CB	Notation in CE	Notation in CC
1.	h_{11}	h_{ib}	h_{ie}	h_{ic}
2.	h_{12}	h_{rb}	h_{re}	h_{rc}
3.	h_{13}	h_{fb}	h_{fe}	h_{fc}
4.	h_{14}	h_{ob}	h_{oe}	h_{oc}

Long & Short Questions

Q.1. Explain the meaning of h-parameter of a transistor . Write down all h- parameters in different configurations. How will you obtain h- parameter of a transistor in CE configuration with the help of the characteristic curves ? [Kanpur 2014,16]

Or

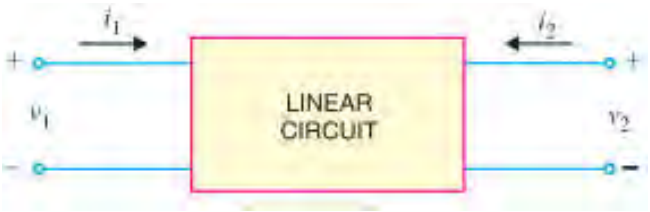
What do you understand by hybrid parameters of a transistor ? [Important]

Or

What is the significance of hybrid parameters ? Define them. How they are determined ?

Every linear circuit having input and output terminals can be analyzed by four parameters (one measured in ohm, one in mho and two dimensionless) called hybrid or h Parameters. Hybrid means "mixed". Since these parameters have mixed dimensions, they are called hybrid parameters.

Consider a linear circuit shown in figure. This circuit has input voltage & current labeled v_1 & i_1 and output voltage & current as v_2 & i_2 .



Hear both the inputs are assumed to flow into the

box.

Determination of h- parameters

From the advance circuit theory voltages and currents in figure can be related by the following set of equations :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2 \qquad \ldots\ldots\ldots \text{(i)}$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \qquad \ldots\ldots\ldots \text{(ii)}$$

- If we short- circuit the output terminals, we have $v_2 = 0$

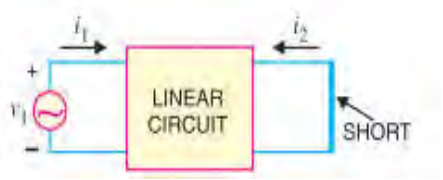
  Applying these changes in above equations we have

$$v_1 = h_{11}\, i_1 + h_{12} \times 0$$

$$i_2 = h_{21}\, i_1 + h_{22} \times 0$$

$$\therefore \quad h_{11} = v_1 / i_1 \text{ for } v_2 = 0$$

$$h_{21} = i_2 / i_1 \text{ for } v_2 = 0$$



- If we open the input terminals, we have $i_1 = 0$

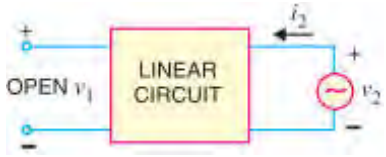
  Applying these changes in above equation (i) & (ii) we have

$$v_1 = h_{11} \times 0 + h_{12} v_2$$

$$i_2 = h_{21} \times 0 + h_{22} \times v_2$$

$$\therefore \quad h_{12} = v_1 / v_2 \text{ for } i_1 = 0$$

$$h_{21} = i_2 / v_2 \text{ for } i_1 = 0$$



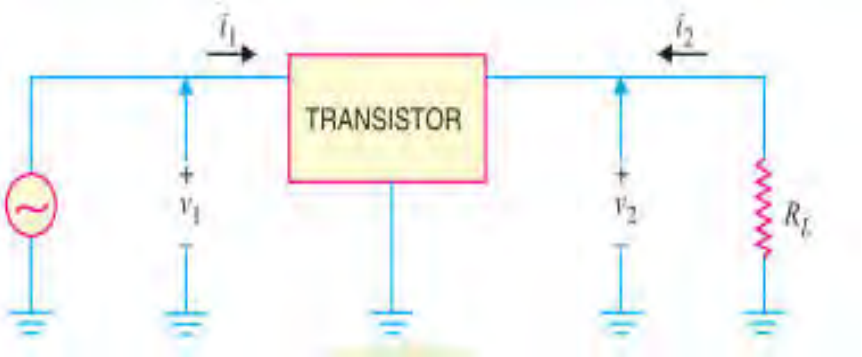
Q.2. Define h- parameter for different configuration of a transistor . How are these determined experimentally ? Draw the hybrid equivalent circuit for any one configuration .

[Kanpur 2015]

For definition refer to Q.1.

Hybrid equivalent circuit of a transistor

For small a.c. sigals, the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal. Under such circumstances, the a.c. operation of the transistor can be described in terms of h



parameters.

- To describe the external behavior of transistor amplifier four quantities are required , these are v_1, i_1, v_2 and i_2 .These voltage & current are related as the following equations :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2 \qquad \text{……. (i)}$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \qquad \text{……. (ii)}$$

- The values of h parameters of a transistors will depend upon the transistor connection (i.e. CB , CE or CC) used.
- The values of h- parameters depend upon the operating point. If the operating point is changed , parameter values also changes.
- The notation v_1 ,i_1, v_2 and i_2 are used for general circuit analysis. In a transistor amplifier, we use the notation depending upon the configuration in which transistor is used. Thus for CE arrangement.

  $v_1 = V_{be}$; $i_1 = I_b$; $v_2 = V_{ce}$; $i_2 = I_c$.

  Here V_{be}, I_b , V_{ce} & I_c . are the rms values .

Nomenclature for Transistor h Parameters

S. No.	h parameter	Notation in CB	Notation in CE	Notation in CC
1.	h_{11}	h_{ib}	h_{ie}	h_{ic}
2.	h_{12}	h_{rb}	h_{re}	h_{rc}
3.	h_{13}	h_{fb}	h_{fe}	h_{fc}
4.	h_{14}	h_{ob}	h_{oe}	h_{oc}

Transistor Circuit Performance in hParameters

(i) **Input impedance** : The general expression for input impedance is

$$Z_{in} = h_{11} - (h_{12}h_{21})/(h_{22} + 1/r_L)$$

For CE Configuration

$$Z_{in} = h_{ie} - (h_{re}h_{fe})/(h_{oe} + 1/r_L)$$

Similarly , expressions for input impedence in CB & CC arrangements can be written.

(ii) **Current gain :** The general expression for current gain is

$$A_i = h_{21}/(1+h_{22}r_L)$$

For CE Configuration

$$A_i = h_{fe}/(1+h_{oe}r_L)$$

(iii) **Voltage gain :** The general expression for voltage gain is

$$A_V = -h_{21} / [Z_{in}(h_{22} + 1/ r_L)]$$

For CE Configuration

$$A_V = -h_{fe} / [Z_{in}(h_{oe} + 1/ r_L)]$$

(iii) Output impedance : The general expression for output impedance is

$$Z_{out} = [h_{22} - h_{21}.h_{12} / h_{11}]^{-1}$$

For CE Configuration

$$Z_{out} = [h_{oe} - h_{fe}.h_{re} / h_{ie}]^{-1}$$

Q.3. Explain two Port network & Y-parameters of a transistor.

Related Short Answer Questions

(i) Explain Y-parameter of a transistor . [Kanpur 2014]

Two port network explained in Q- 1 & Q-2

Admittance parameters or Y-parameters are the properties used in many areas of electrical engineering, such as power, electronics, and telecommunications. These parameters are used to describe the electrical behavior of linear electrical networks. They are also used to describe the small-signal (liberalized) response of non-linear networks.

The equations describing admittance parameters are

$$I_1 = y_{11}V_1 + y_{12}V_2$$

$$I_2 = y_{21}V_1 + y_{22}V_2$$

- If we short- circuit the output terminals, we have $v_2 = 0$

  Applying these changes in above equations we have

  $$I_1 = y_{11}V_1 + y_{12} \times 0$$

  $$I_2 = y_{21}V_1 + y_{22} \times 0$$

  $\therefore$ $y_{11} = v_1 / i_1$ for $v_2 = 0$

  $y_{21} = i_2 / v_1$ for $v_2 = 0$

- If we short the input terminals, we have $v_1 = 0$

  Applying these changes in above equation (i) & (ii) we have

  $$I_1 = y_{11} \times 0 + y_{12}V_2$$

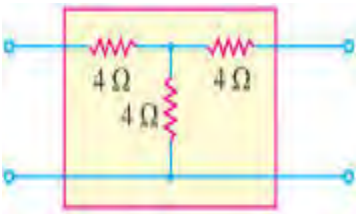
$I_2 = y_{21} x0 + y_{22} V_2$

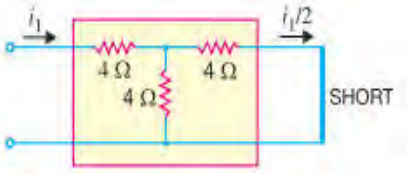
$\therefore \quad y_{12} = I_1 / v_2$ for $i_1 = 0$

$y_{22} = i_2 / v_2$ for $i_1 = 0$

Numerical

Q.1. Find the h- parameters of the circuit shown





Exp: Considering all the output terminals to be shorted , the input impedance under this condition is the parameter h_{11}

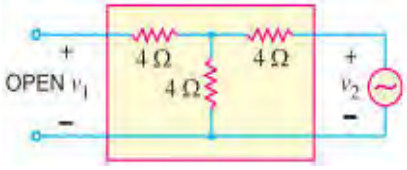
$\therefore h_{11} = 4 + 4 \;||\; 4 = 4 + 4.4/(4+4) = 6\Omega$

$\because$ Input current i_1 will be divided equally between ll connected resitances

$\therefore i_2 = -i_1/2 = -0.5 i_1$

$\because h_{21} = i_2 / i_1$

$\therefore h_{21} = i_2 / i_1 = -0.5\, i_1 / i_1 = -0.5$



In order to find h_{12} & h_{22} , with input open circuited we have

Under this condition , we have $v_1 = 4\,\Omega \,.\, V_2 / (4\,\Omega + 4\,\Omega) = 0.5 \times V_2$

$\because h_{12} = v_1 / v_2 = 0.5\, i_1 / i_1 = 0.5$

Looking into the output terminals with input terminals open, the output impedance is 8 Ω

$\therefore h_{22} = 1/8 = 0.125$ mho

Q.2. Figure shows the transistor amplifier in CE arrangement. The h parameters of transistor are as under :

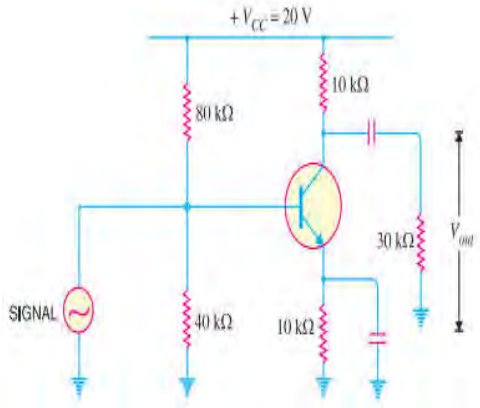
$h_{ie} = 1500\,\Omega$; $h_{fe} = 50$; $h_{re} = 4 \times 10^{-4}$; $h_{oe} = 5 \times 10^{-5}$ mho

Find (i) a.c. input impedance of the amplifier

(ii) voltage gain

(iii) output impedance.

Exp: The a.c. load r_L seen by the transistor is equivalent of the parallel combination of RC(= 10 kΩ & RL= 30 kΩ i.e. $r_L = 10 \times 30 / (10 + 30) = 7.5$ k Ω



(i) The input impedance looking into the base of transistor is given by :

$Z_{in} = h_{ie} - (h_{re}h_{fe})/ (h_{oe} + 1/ r_L)$

Putting the respective values

$$Z_{in} = 1390\ \Omega$$

(ii)

Voltage gain i.e. $A_V = -h_{21}/ [Z_{in}(h_{22} + 1/ r_L)]$

Putting the respective values

$$A_V = -196$$

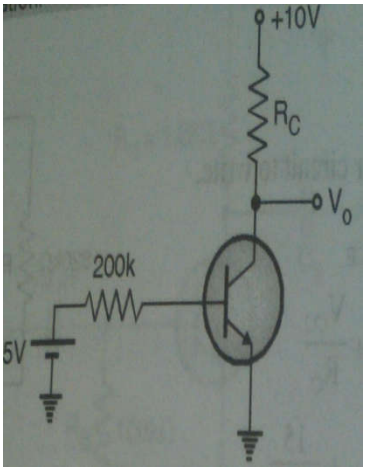
(iii) Output impedance i.e. $Z_{out} = [h_{oe} - h_{fe}.h_{re}/ h_{ie}]^{-1}$

Putting the respective values

$$Z_{out} = 5.88\ K\ \Omega$$

Q.3. A silicon transistor with $V_{BE(sat)} = 0.8$ V , $\beta = h_{FE} = 100$, $V_{CE(sat)} = 0.2$ V is used in the circuit shown. Find the minimum value of R_C for which the transistor remains in saturation .

Exp: Given $V_{BE(sat)} = 0.8$ V , $\beta = h_{FE} = 100$ & $V_{CE(sat)} = 0.2$ V



Applying KVL at the input terminal , we have

$-5V + 200k.\ I_B + 0.8V = 0$

$\therefore I_B = 4.2/ (200 \times 10^3) = 21\mu A$

$\because I_C = \beta\ I_B = 100 \times 21\mu A = 2.1mA$

Applying KVL at the output terminal , we have

$-10 + R_C\ I_C + V_{CE(sat)} = 0$

$\therefore R_C = (10 - 0.2) / 2.1mA = 4.667k\Omega$ Ans

Chapter-6
Small signal Amplifier

AC Models

A model is the combination of circuit elements , properly chosen, the best approximates the actual behavior of a semiconductor device under specific operating conditions.

The ac equivalent of a network is

1. Setting all dc sources to zero and replacing them by a short- circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent.
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 & 2.
4. Redrawing the network in a more convenient and logical form.

After a transistor has been biased with the Q point near the middle of load line, we can couple a small ac voltage into the base. This will produce an amplified ac collector voltage. The invention of amplifying devices was crucial to the evolution of electronics.

Base- Biased Amplifier

Good coupling occurs when the reactance of the coupling capacitor is much smaller than the resistance at the lowest frequency of the ac source. In a base-biased amplifier, the input signal is coupled into the base. This produces an ac collector voltage. The amplified and inverted ac collector voltage is than coupled to the load resistance.

Emitter Biased Amplifier

Good bypassing occurs when the reactance of the coupling capacitor is much smaller than the resistance at the lowest frequency of the ac source. The bypassed point is an ac ground. With either a VDB or a TSEB amplifier, the ac signal is coupled into the base. The amplified ac signal is then coupled to the load resistance.

Small- signal operation

The ac base voltage has a dc component and an ac component. These set up dc and ac components of emitter current. One way to avoid excessive distortion is to use small-signal operation. This means keeping the peak- to- peak ac emitter current less than $1/10^{th}$ of the dc emitter current.

AC Beta

The ac beta of a transistor is defined as the ac collector current divided by the ac base current. The values of the ac beta usually differ only slightly from the values of the dc beta. On data sheets, h_{FE} is equivalent to β_{dc} and h_{fe} is equivalent to β.

AC Resistance of the emitter diode

The base-emitter voltage of a transistor has a dc component V_{BEQ} and an ac component V_{be} . The ac base-emitter voltage sets up an ac emitter current of i_e. The ac resistance of the emitter diode is defined as v_{be} divided by i_e.

Two Transistor Models

As far as ac signal are concerned, a transistor can be replaced by either of two equivalent circuits : The π model or the T model. The π model indicates that the input impedence of the base is $\beta r'_e$.

Analyzing an amplifier

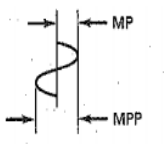
The simplest way to analyze an amplifier is to split the analysis into two parts : a dc analysis and an ac analysis. In the dc analysis, the capacitor are shorted and the dc supply points are ac grounds.

Class A & B operation

In a Class A amplifier transistor operates in the active region at all times. This implies that current in the output circuit flows at all times.

In a class B operation, the collector current flows for only half the cycle (180^0). In this operation Q point is located at cutoff.

Maximum Peak- to -Peak



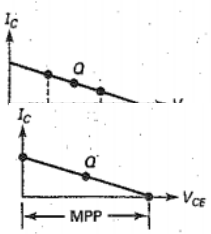
MPP= 2MP

Output Power

$P_{out} = \frac{V_{out}^2}{8R_L}$

Maximum power output

$P_{out(max)} = \frac{MPP^2}{8R_L}$



Effect of temperature

An increase in temperature produces an increase in the minority carrier current, but negative change in V_{BE}. These effects leads to an increase in collector current with temperature.

Heat sinks

One way to increase the power rating of a transistor is to get rid of the heat faster. This is why heat sinks are used. If we increase the surface area of the transistor case, we allow the heat to escape more easily into the surrounding air.

Thermal resistance

Thermal resistance is the ability of a material to resist flow of heat . Thermal resistivity is the reciprocal of thermal conductivity and can be expressed as

Distortion in Amplifier

When the Q point is at the centre of the dc load line, the ac signal cannot use all the ac load line without clipping. For instant, if the ac signal increases, we get distorted output i.e. cutoff clipping If a Q point is moved higher , a large signal will drive the transistor into saturation with saturation clipping or distorted output. When a distorted output derives loudspeaker sounds terrible.

Cascading of stages

To get more voltage gain , amplifier stages are cascaded i.e. output of first stage as the input to second stage & the output of second stage can be used for input to third stage.

Multistage Amplifier

The overall voltage gain equals the product of the individual voltage gains. The input impedance of second stage is the output impedance of first stage.

Frequency response

The frequency response of an amplifier is the graph of its gain versus the frequency. An ac amplifier has lower & upper cutoff frequency. Coupling & bypass capacitors produce the lower cutoff frequency. Internal transistor capacitance & stray wiring capacitances produces upper cutoff frequency.

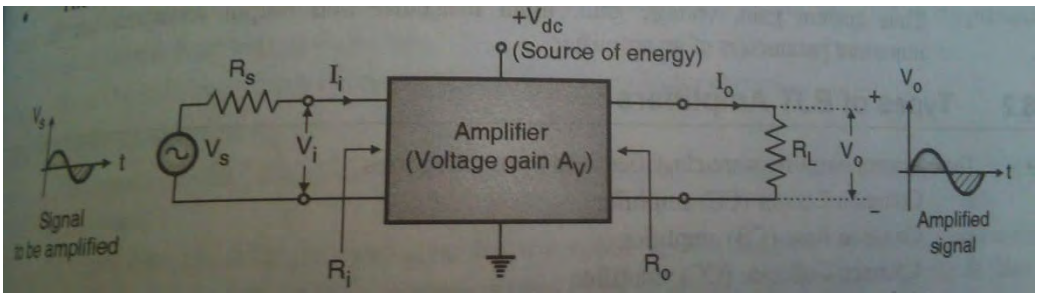
Negative & Positive feedback in transistor amplifiers

The process of returning partial part of output signal back to input circuit is called feedback. Positive feedback is also known as regenerative, as feedback part is added to input. Negative feedback also known as degenerative in which partial part of output signal feed to input is subtracted.

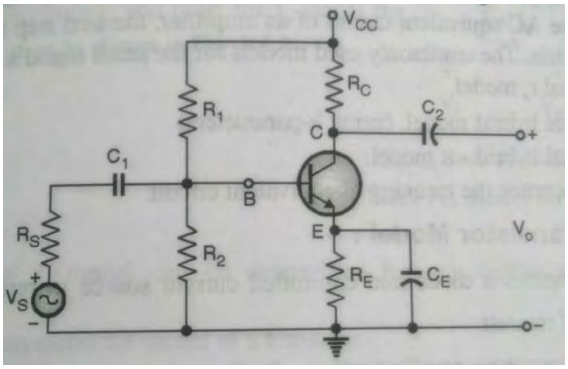
Long & Short Questions

Q.1. What is Amplifier ? Describe the principle operation of a amplifier with the help of neat block diagram. What are its types & various application of Amplifier?

Amplifier are meant to amplify the analog signals. The amplifier is supposed to multiply the input signal by a constant to produce the output. This multiplier is grater then one and called as "gain" of the amplifier.



- In order to amplify the input signal V_S , all the amplifier needs a dc power supply i.e. $+V_{dc}$
- The amplifier should contain at least one active device such as BJT, FET or OP-AMP . If BJT used must be biased in the active region.



VDB amplifier

Types of BJT Amplifier

The types of amplifier are classified into three categories :

1. Common Emitter (CE) amplifier
2. Common Base (CB) amplifier
3. Common Collector (CC) amplifier

BJT is used

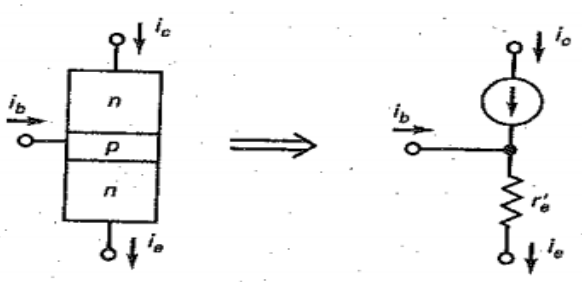
1. As buffer amplifier
2. For the impedance matching
3. As the output stage(Power amplifier)

Q.2. What are different transistor models ? Analyze Amplifier using any model.

To analyze the ac operation of a transistor amplifier, we need an ac equivalent circuit for a transistor. In order words we need a model for the transistor that simulates how it behaves when an ac signal is present.

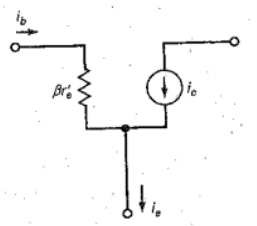
The T Model

One of the earliest models was the Ebers- Moll model as shown in fig. As far as a small ac signal is concerned, the emitter diode of a transistor acts like an ac resistance r'_e and the collector diode acts like a current source i_c. Since the Elbers- Moll model looks like a T on its side, the equivalent circuit is also called the **T model**



The π Model

Fig shows a π Model of a transistor , is easier to use then T model because the input impedence is not obvious in T model. π Model clearly shows that an input impedence of $\beta r'_e$ will load the ac voltage source driving the base.

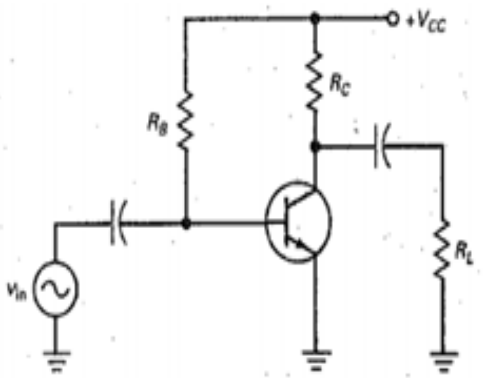


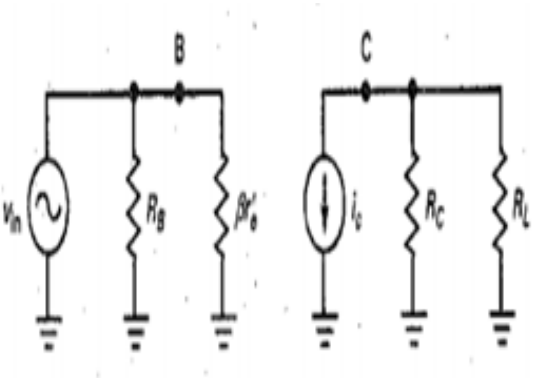
Analysig an Amplifier

Since the π & T models are ac equivalent circuits for a transistor, we can use either one when analyzing an amplifier.Amplifier action is the superposition of ac & dc effect.

The Transistor Equivalent Circuit

The equivalent circuit of amplifier is shown in figure , all the capacitors have been shorted , the dc supply point has become ac ground , and the transistor has been replaced by its π Model. In the base circuit , the ac input voltage appers across R_1 in parallel with R_2 in parallel with $\beta r'_e$.In the collector circuit , In the collector circuit , the current source pumps an ac current of i_C through R_C in parallel with R_L .





Q.2. Explain working of two supply emitter bias amplifier with the help of neat block diagram.

Due to biasing i.e. TSEB

$V_B \approx 0V$

$V_B = -0.7V$

$V_C = 5.32$ V

$I_C = 1.3$ mA

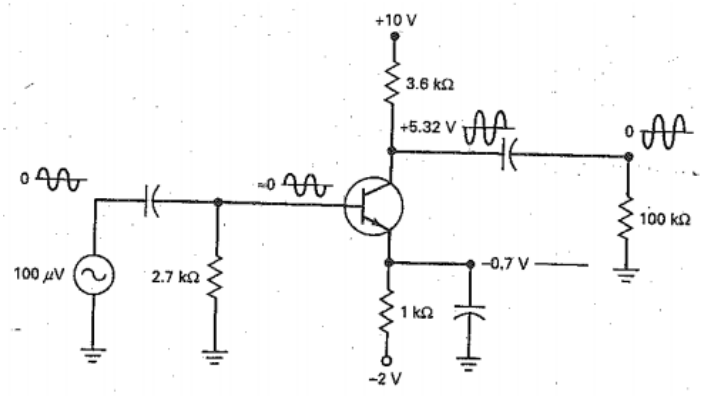


Fig. shows two coupling capacitors and an emitter bypass capacitor. The input signal is coupled into base and the signal is amplified that is coupled to the load.

Waveforms : The ac source voltage is a small sinusoidal voltage . The base voltage has a small ac component riding on the dc component of approx. 0V. The total collector voltage is an inverted sine wave riding on the dc collector voltage of +5.32V. The load voltage is the same amplified signal with no dc component.
Due to bypass capacitor there is pure dc voltage across emitter. If the bypass capacitor is open , an ac voltage appears across emitter that greatly reduces the gain of amplifier.

Q.3. Define AC resistance of Emitter diode.

The ac resistance of emitter diode is defined as the $r'_e = \frac{V_{be}}{i_e}$

With the solid state physics and calculus , it is possible to derive the formula for the ac emitter resistance. $r'_e = \frac{25mV}{I_E}$

Where I_E = DC emitter current.

Q.4. Define AC Beta & relationship between r and h parameters

The ac current gain is known as AC Beta i.e. $\beta = \frac{i_c}{i_b}$. For convenience we use capital letter & subscripts for dc and small letters for ac quantities.

Relationship

AC Beta, $\beta = h_{fe}$

AC resistance, $r'_e = \frac{h_{ie}}{h_{fe}}$

Q.5. Find the expression for voltage gain of Amplifier

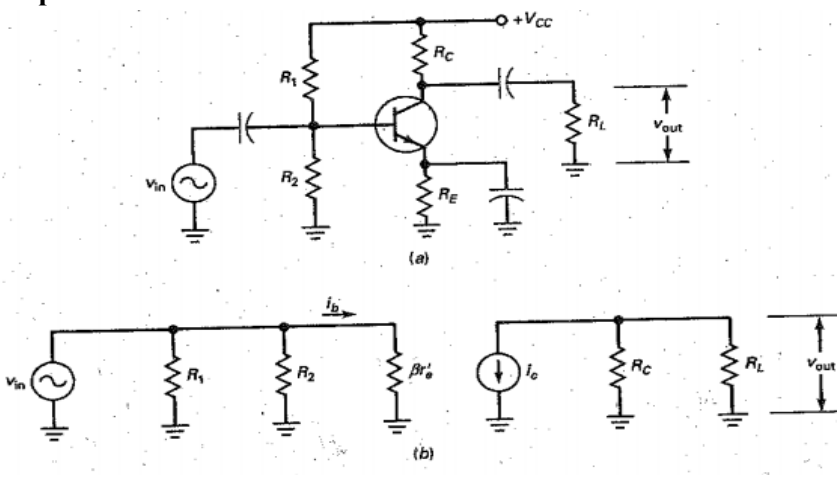


Fig. (b) shows the ac equivalent circuit of the amplifier circuit in fig. (a) ,using the π model of the transistor. The ac base current i_b flows through the **input impedance** of the base ($\beta r'_e$).

With Ohm's law, we have

$\mathbf{v_{in}} = i_b \beta r'_e$

In the collector section , the current source pumps i_c trough the parallel connection of R_C & R_L. Therefore, the ac output voltage equals:

$\mathbf{v_{out}} = i_c(R_C \parallel R_L) = i_b \beta(R_C \parallel R_L)$

Therefore **Voltage gain** i.e.

$\mathbf{A_V} = \frac{v_{out}}{v_{in}} = [\, i_b \beta(R_C \parallel R_L)] \,/\, i_b \beta r'_e$

$= (R_C \parallel R_L) / \; r'_e$

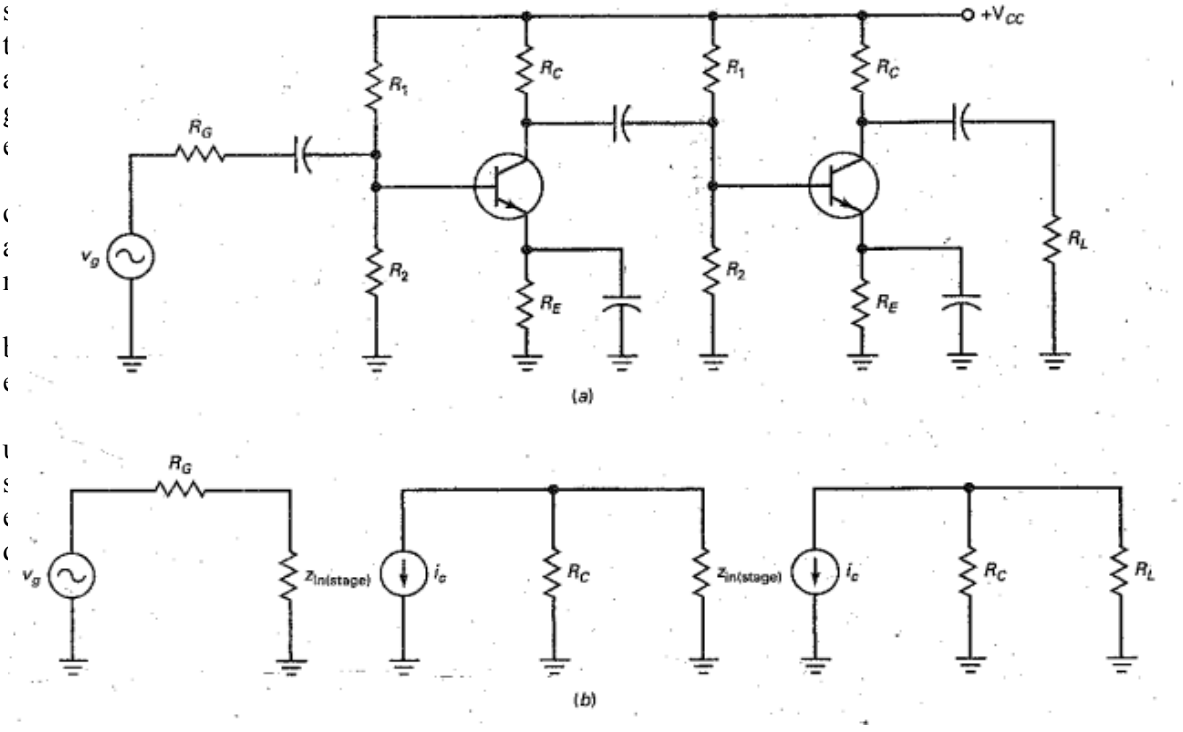
If $\mathbf{r_c} = (R_C \parallel R_L)$, the $A_V = r_c / r'_e$

The **input impedance** is $\mathbf{z_{in}} = R_1 \parallel R_2 \parallel \beta r'_e$

If the input source has internal resistance of $\mathbf{R_G}$, then $\mathbf{v_{in}} = \frac{z_{in}}{R_G + z_{in}} v_S$

Q.6. What are multistage amplifier ? Find the expression for voltage gain. [Kanpur 2016]

To get more voltage gain, we can create multistage amplifier by cascading two or more amplifier stages**.** This means using the output of the first stage as the input to a second stage The output of the second



as the input to the third stage and so on.

Voltage Gain of first stage

With the equivalent circuit shown in fig. b . The ac collector resistance of the first stage is

First stage : $r_c = R_C \;||\; z_{in(stage)}$

The voltage gain of the first stage is :

$$A_{v_1} = R_C \;||\; z_{in(stage)} / r'_e$$

Voltage Gain of second stage

The ac collector resistance of the second stage is:

Second stage : $r_c = R_C \;||\; R_L$

& the voltage gain is :

$$A_{v_2} = [R_C \;||\; R_L] / r'_e$$

Total voltage gain

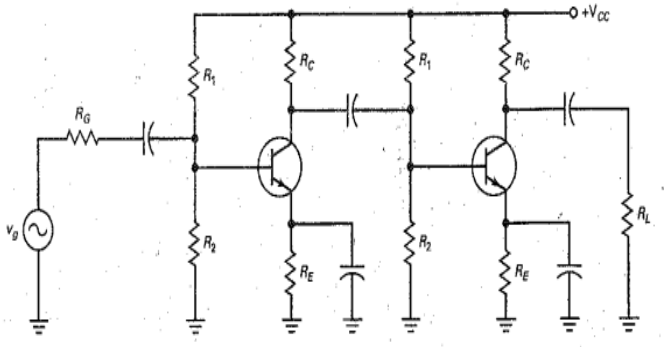
The total voltage gain of the amplifier is given by the product of the individual gains :

$$A_v = A_{v_1} . A_{v_2}$$

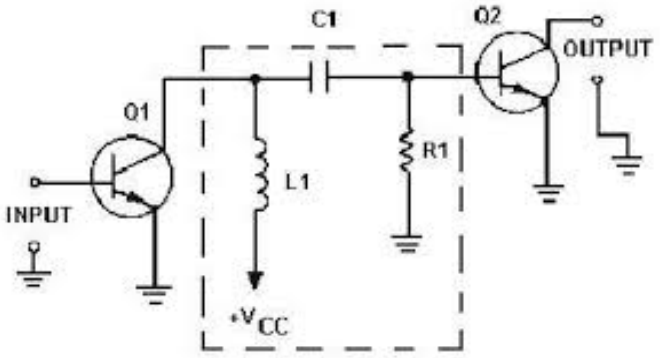
Q.7. What do you mean by amplifier coupling ? [Kanpur 2013]

The process of transferring signals from one stage to other via a medium without any loss know as coupling. Some of the famous coupling are

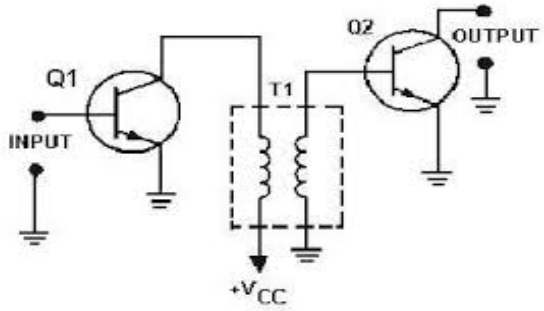
1. RC coupling



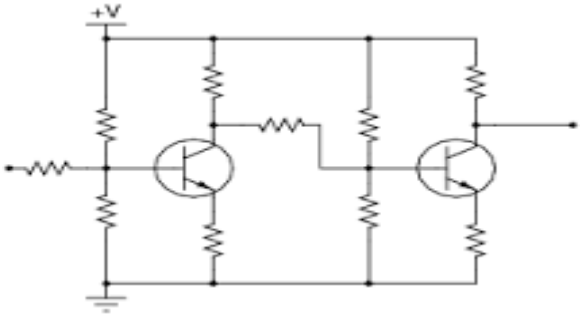
2. Impedance Coupling



3. Transformer coupling



4. Direct coupling (DC)



Q.8. Explain the working of a RC coupled amplifier in common emitter configuration . Draw its frequency response curve [Kanpur 2012]

Or

Draw circuit of a two-stage RC coupled CE amplifier. Explain with reasons what factors affect the gain of the amplifier at low and high frequencies? [Important]

Or

Draw a circuit diagram of a two-stage RC coupled amplifier in common emitter configuration and explain its working . [Kanpur 2014]

Refer to Q. 6

Effects of gain of the amplifier at low and high frequencies

The frequency response of an amplifier is the graph of its gain versus the frequency. An ac amplifier has lower & upper cutoff frequency. Coupling & bypass (fig. b)capacitors produce the lower cutoff frequency. Internal transistor capacitance & stray wiring capacitances (fig. b) produces upper cutoff frequency.

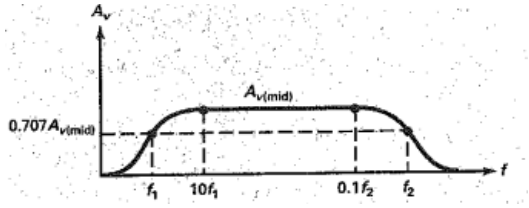


fig. (a)

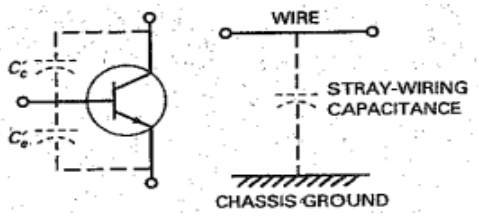


fig. (b)

Fig. (a) shows the frequency response of an amplifier. In the middle range of frequencies, the voltage gain is maximum. At low frequencies, the voltage gain decreases because the coupling and bypass capacitor no longer act like short circuits. Instead, their capacitive reactances are large enough to drop some of the ac signal voltage.

The approximation for calculating gain $A_v = \frac{A_{v(mid)}}{\sqrt{1+(\frac{f_1}{f})^2} \cdot \sqrt{1+(\frac{f}{f_2})^2}}$.

Loading effects of input impedance

Loading effects occurs when amplifiers are cascaded. Due to cascading of amplifier , the output resistance of previous stage decreases due to which , gain of amplifier decreases.

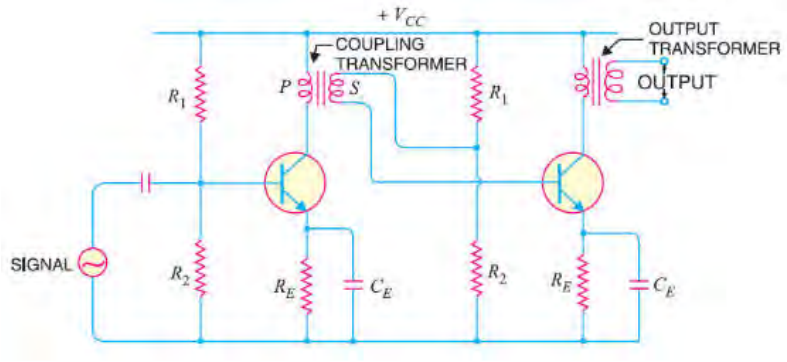
Q.9. Draw the circuit diagram of a transformer coupled transistor. Derive the expression for voltage gain at low, mid and high frequency . [Kanpur 2013]

Transformer Coupled Transistor Amplifier

In case of a RC coupled transistor amplifier the voltage and power gain are low since, the effective load resistance of each stage is decreased due to the low resistance presented by the input of each stage to the next stage. If the effective load resistance of each stage could be increased, the voltage and power gain could also be increased. This can be achieved by **transformer coupling.**

- By using the impedance matching properties of transformer, the low resistance of one stage or load can be reflected as a high load resistance to the previous stage.
- Transformer coupling is normally used when the load is small. It is mostly used for power amplification.

Working of Transformer Coupled Transistor Amplifier



As shown in the above fig. a coupling transformer is used to feed the output of one stage to the input of the next stage. The primary P of this transformer is made the collector load and its secondary S supplies input to the next stage.
When an a.c. signal is applied to the base of first transistor, it appears in the amplified form across the primary P of the coupling transformer.
Now the voltage developed across P is transferred to the input of the next stage by the transformer secondary S.
The second stage now performs the amplification in an exactly same manner.

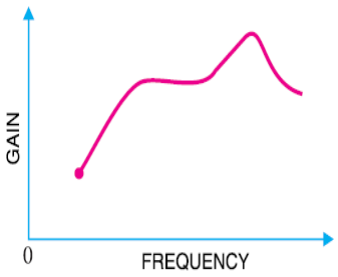
Voltage gain

$$A_{v_1} = \frac{r_{0.1}}{r_{e.1}}, where, r_{0.1} = a^2\, r_{i.2}$$

Where a= N_1/ N_2 for T_1 $r_{i.2} = R_1 \;||\; R_2 \;||\; \beta_2 r_{e.2}$ {R_1, R_2 of 2nd stage}

Similarly , $A_{v_2} = \frac{r_{0.2}}{r_{e.2}}$ $where, r_{0.2} = a^2\, r_{i.1}$

Frequency Response of Transformer Coupled Transistor Amplifier



- The frequency response of a transformer coupled amplifier is shown in the figure. It is clear from the above fig. that its frequency response is poor than the RC coupled amplifier. The gain is constant only over a small range of frequency.
- Since, the output voltage is equal to the collector current multiplied by reactance of primary, hence at low frequencies, as the reactance of primary begins to fall , the output voltage also decrease and hence the gain.
- At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence the gain.
- Due to these two factors, there is disproportionate amplification of frequencies in a complete signal such as music, speech etc. Hence, transformer coupled amplifier introduces frequency distortion.

Advantages of Transformer Coupled Transistor Amplifier

1. There is no loss of signal power in the collector or base resistors.
2. An excellent impedance matching can be achieved in a transformer coupled amplifier.

3. Due to excellent impedance matching, transformer coupling provides higher gain. A properly designed single stage transformer coupling can provide the gain of two stages of RC coupling.

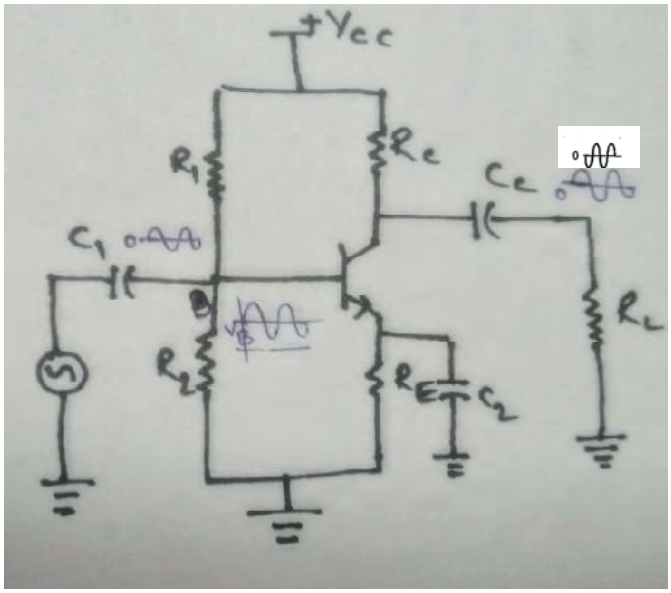
Disadvantages of Transformer Coupled Transistor Amplifier

1. It has a poor frequency response.
2. The coupling transformers are bulky and expensive at audio frequencies.
3. Frequency distortion is higher i.e. low frequency signals are less amplified as compared to the high frequency signals.
4. Transformer coupling introduces hum in the output.

Q.10. Show that the output voltage of a single stage common emitter transistor amplifier is 180^0 out of phase with input voltage . [Important]

Or

What is single stage transistor amplifier ? [Important]



When only one transistor is used in amplifier to amplify the signal is known as single stage amplifier as shown in figure.
In fig. the voltage beyond B point is AC type due to the capacitor C_1.
Due to voltage divider biasing ,the ac input voltage superimpose on dc voltage V_B , keeping base-emitter terminal always forward bias.

$v_{out} = V_{cc} - i_c R_C$
$= V_{cc} - \beta i_b R_C$ { since , $i_c = \beta i_b$}

Now when i_b will be at maximum, i_c will be at maximum i.e. magnitude of $i_c R_C$ will be maximum . It means maximum subtraction from V_{CC} and therefore minimum v_{out} .

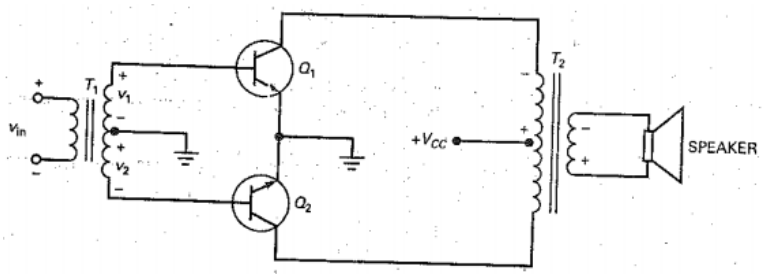
when i_b will be at minimum i_c will be at minimum i.e. magnitude of $i_c R_C$ will be minimum . It means minimum subtraction from V_{CC} and therefore maximum v_{out} . This happens sinusoidally & this practice is periodic in nature.
Therefore the output voltage is 180^0 out of phase w.r.t. input as shown in above fig.

Q. 11. Draw the circuit of push-pull class B audio "Power amplifier". Derive an expression for the efficiency of the amplifier. What are the advantages of push- pull amplifier ? [Kanpur 2014]

Class A is the Common way to run a transistor in linear circuits because it leads to the simplest and most stable biasing circuits. But Class A is not most efficient way to operate a transistor .This need introduces class B operation of power amplifier.

Push –Pull Circuit

Fig. shows a basic class B amplifier. When the transistor operates as class B, it clips off half a cycle (there is no any biasing circuit), To avoid the resulting distortion , two transistors are used in a push-pull arrangement. Push –Pull means that one transistor conducts for half a cycle while the other is off and vice versa.



Operation

- On positive half cycle of input voltage , the secondary winding of T_1 has voltage v_1 & v_2 as shown.
- Therefore the upper transistor conducts and the lower one cuts off. The collector current through Q_1 flows through the upper half of the output primary winding.
- This produces an amplified and inverted voltage, which is transformer-coupled to the loudspeaker.
- On the next half cycle of input voltage , the polarities reversed . Now , the lower transistor turn on and the upper transistor turns off . The lower transistor amplifies the signal, and the alternate half cycle appears across the loudspeaker.
- Since each transistor amplifies one-half of the input cycle, the load-speaker recives a complete cycle of the amplified signal

For derivation refer to Q.9.

Advantages

- No bias circuit is needed
- Improved efficiency , the maximum efficiency is 78.5 %, so class B push-pull amplifier is more commonly used for an output stage then a class A power amplifier

Disadvantages

The main disadvantage of amplifier is the use of transformer , making it bulky & expensive

Q. 12. Explain the principle of a feedback amplifier. What are positive and negative feedbacks? [Kanpur 2012]

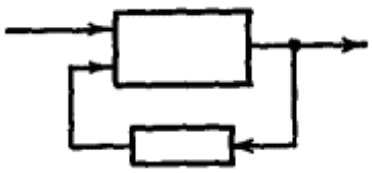
Or

What is the principle of feedback? Establish the relation between voltage gains of a common amplifier and a feedback amplifier. [Kanpur 2014,15]

Or

What is meant by feedback in amplifier? Define negative & positive feedback . Explain how negative feedback in an amplifier helps in improving gain stability and reducing the distortion. [Kanpur 2016]

Suppose a small voltage is fed back from the output of an amplifier to its input as in fig.



If this voltage is in the same phase (crest for crest, trough for trough) as the input or signal voltage, the feedback is said to be positive or *regenerative* and the circuit will likely go into

oscillation.

If the voltage is in reverse phase (crest for trough of the wave-form), the feedback is negative or *degenerative.*

Let the amount of the feedback voltage be a fraction *(F)* of the output voltage *E*. Then the actual input will be *FE* plus the original signal e. The output voltage is equal to the actual input voltage multiplied by the voltage amplification *A*.

Thus $E = A(e + FE)$. Solving this equation for the effective amplification or gain of a feedback amplifier, we find

$$G = E/e = \frac{A}{1-FA} = -\frac{1}{F}\left(\frac{1}{1-\frac{1}{FA}}\right)$$

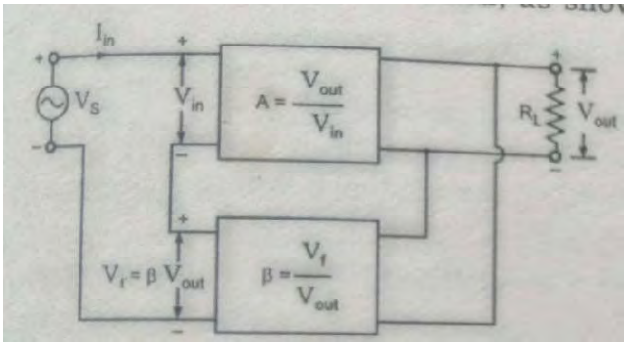
When *F* is positive, the circuit is regenerative, and vice versa. When the " feedback factor " *FA* is very large, the gain becomes $(— 1/F)$, and the effective amplification is independent of the gain *A* of the amplifier alone. This means that, with degenerative feedback, the amplifier will have *great stability,* retaining its overall voltage gain at a constant value for long periods of time despite appreciable changes in battery voltages, temperature, and mechanical vibration.

Degenerative feedback *reduces harmonic distortion* arising in the amplifier. This is because the distortion is fed back and is itself degenerated.

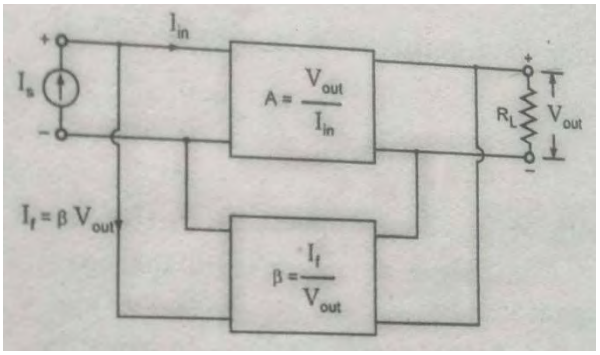
Basic negative feedbacks.

Negative feedback are generally of four types

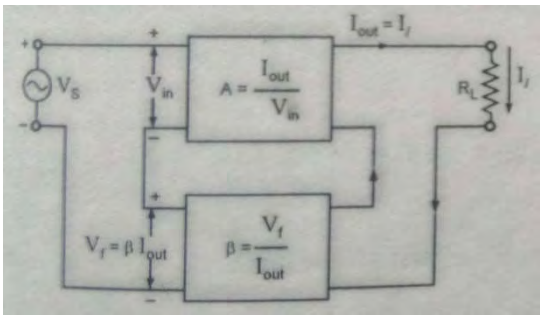
Voltage series feedback



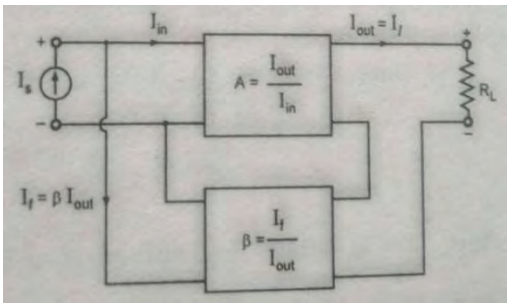
Voltage shunt feedback



Current series feedback

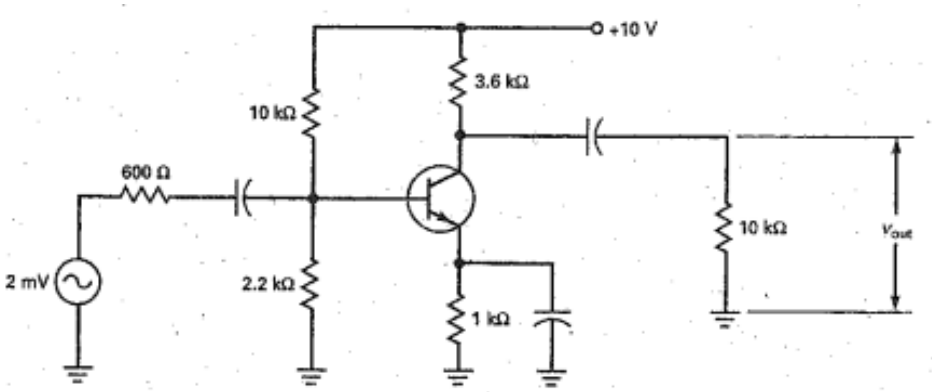


Current shunt feedback



Numerical

Q.1. Calculate amplifier gain , if β= 300 ?



Exp: V_E = 2.2 k Ω x 10V/ (2.2 k Ω+10 k Ω) -0.7V = 1.103V

I_E= V_E/ R_E = 1.103V/ 1 k Ω = 1.103mA

∴ r_e = 25mV/ I_E = 25mV/1.103mA = 22.66 Ω

∵ $r_c = R_C$ ׀׀ R_L

∴ r_c = 3.6 k Ω ׀׀ 10k Ω = 2.65 k Ω

∵ $A_V = r_c / r'_e$

$\therefore A_V = 2.65\ k\Omega / 22.66\ \Omega = 116.94$ Ans

Q.2. The ac generator has an internal resistance of 600Ω for the amplifier in Q.1. What is the output voltage , if β= 300 ?

Exp: As calculated above $r_e = 22.66\ \Omega$, $A_V = 116.94$

When β= 300 , the input impedance is z_{in}

$\mathbf{z_{in}} = R_1 \ \| \ R_2 \ \| \ \beta r'_e$

$\therefore \mathbf{z_{in}} = 10k\ \Omega \ \| \ 2.2\ k\Omega \ \| \ 300 \times 22.66\ \Omega$

$= 10k\ \Omega \ \| \ 2.2\ k\Omega \ \| \ 6.798k\ \Omega = 1.42k\ \Omega$

$\because \mathbf{v_{in}} = \frac{z_{in}}{R_G + z_{in}} v_s$

$\therefore \mathbf{v_{in}} = 1.42\ k\Omega \times 2mV / (600\ \Omega + 1.42\ k\Omega) = 1.41mV$

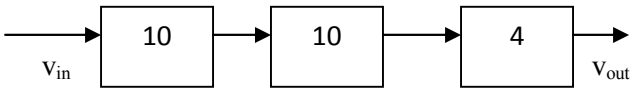
$\because v_{out} = A_V\ v_{in}$

$\therefore v_{out} = 116.94\ k\Omega / 1.41mV = 165mV$ Ans

Q.3. The value of r.ms. voltage of the input signal of atree stage RC coupled amplifier is 0.1volt. If the voltage gains of the three stage are 10,10 and 4 resp., what will be the output voltage ?

[Important]

Exp:



Since , gain of three RC coupled amplifier are 10,10 & 4 respectively

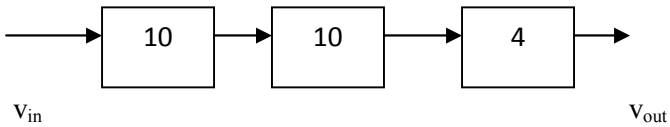
therefore, gain of three cascade system= 10*10*4=400

v_{out}= 0.1*400= 40v

Q.4. A two stage common emitter RC coupling. The voltage gain of each stage is 50 & $R_C = 5k\ \Omega$ for each stage . If input impedance of each stage is 2k Ω , then find the overall voltage gain.

[Important]

Exp:



Since , gain of three RC coupled amplifier are 50,50 & 50 respectively

therefore, gain of three cascade system= 50*50*50=125000 Ans

Q.6. An ac amplifier with a midband voltage gain of 200. If the cutoff frequencies are f_1= 20Hz and f_2 = 20kHz, what does the frequency response look like ? What is the voltage gain if the input frequency response look like ? What is the voltage gain if the input frequency is 5Hz ? If it is 200kHz ?

Exp: In the midband , the voltage gain is 200 . At either cutoff frequency , it equals

A_V= 0.707 (200) = 141

Voltage gain for the an input frequency of 5Hz

$$A_V = \frac{A_{v(mid)}}{\sqrt{1+(\frac{f_1}{f})^2}}$$

$$\therefore A_V = \frac{200}{\sqrt{1+(\frac{20}{5})^2}} = \frac{200}{\sqrt{1+(4)^2}} = \frac{200}{\sqrt{17}} = 48.5$$

Voltage gain for the an input frequency of 200kHz

$$\therefore A_V = \frac{200}{\sqrt{1+(\frac{200}{20})^2}} = 19.9$$

Q.5. A two stage common emitter R-C coupled amplifier uses transistor of the type BC149B, whose hybrid parameter are : h_{fe} =330, h_{ie}= 4.5 kΩ & load resistance R_L= 5.5 kΩ . Find the required value of the coupling capacitor C so that the lower half power frequency is 30Hz.

[Important]

Exp: Given : h_{fe} =330, h_{ie}= 4.5 kΩ, R_L= 5.5 kΩ and f_L= 5.5 kΩ

Since, for two stage RC coupled amplifier the half power frequency , f_L is given by

$$f_L = 1/ [2\pi C_C(h_{ie} + R_L)]$$

$$\therefore C_C = 1/ [2\pi f_L (h_{ie} + R_L)]$$

$$\therefore C_C = 1/ (2x\ 3.14\ x\ 30\ (4.5 + 5.5)x\ 10^3) = 0.53\ x\ 10^{-6} = 0.53\mu F$$ Ans

Chapter-7
Field Effect transistor

JFET

The junction FET, abbreviated as JFET has three terminals a source , gate & drain . The JFET has two diodes: the gate-source diode and the gate-drain diode. For normal operation , the gate –source diode is reverse biased; then , the gate voltage controls the drain current.

Drain Curves

Maximum drain current occurs when the gate-source voltage is zero. The pinchoff voltage separates the ohmic and active regions for V_{GS} =0 . The gate-source cutoff voltage has the same magnitude as the pinchoff voltage. $V_{GS(off)}$ turns the JFET off.

Biasing in the Ohmic region

Gate bias is used to bias a JFET in the ohmic region. When it operates in the ohmic region , a JFET is equivalent to a small resistance of R_{DS}. To ensure operation in the ohmic region , the JFET is driven into hard saturation by using V_{GS}= 0 and $I_{D(sat)} << I_{DSS}$

Biasing in the active region

When the gate voltage is much larger than V_{GS}, voltage divider bias can set up a stable Q point in the active region. When +ve & -ve supply voltages are available , two –supply source bias can used to get a stable Q point. Self-bias is used only with small-signal amplifiers because the Q point is less stable than with the other biasing methods.

Transconductance

Transconductance g_m tells us how effective the gate voltage is in controlling the drain current. The quantity g_m is the slope of the transconductance curve, which increases as V_{GS} approaches zero.

The Transconductance curve

This is a graph of drain current versus gate-source voltage. The drain current increases more rapidly as V_{GS} approaches zero. Because the equation for drain current contains a squared quantity, JFETs are referred to as square-law devices. The normalized transconductance curve shows that I_D equals one-quarter of maximum when V_{GS} equal half of cutoff.

JFET Amplifier

A CS amplifier has a voltage gain of $g_m r'_d$ and produces an inverted output signal. One of the most important uses of a JFET amplifier is the source follower, which is often used at the front end of systems because of its high input resistance.

The JFET Analog Switch

JFET acts like a switch that either transmits or blocks a small ac signal. To get this type of action , the JFET is biased into hard saturation or cutoff, depending on whether V_{GS} is high or low. JFET shunt and series switches are used. The series type has a higher on-off ratio.

MOSFET

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a type of field-effect transistor (FET). It has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals.

The D- MOSFET

The depletion mode MOSFET , abbreviated as D- MOSFET is normally on, has a source , gate and drain. The gate is insulated from the channel. Because of this, the input resistance is very high. The D-MOSFET has limited use, mainly in RF circuits.

The E- MOSFET

The Enhancement mode MOSFET is abbreviated as E- MOSFET is normally off. When the gate voltage equals the threshold voltage, an n-type inversion layers connects the source to the drain. When the gate voltage is much greater than the threshold voltage , the device conducts heavily.

MOSFET Preamplifier

MOSFET is an amplifying device in which the output current depends on the input voltage. The MOSFET Pre Amplifier is a sensitive and stable Preamp circuit using an N-Channel MOSFET and a PNP Bipolar transistor. This combination gives high input impedance and low output impedance with stabilized gain.

MOSFET Uses

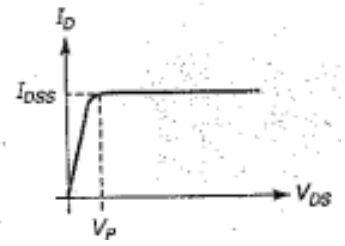
The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices. The MOSFET is very far the most common transistor and can be used in both analog and digital ckt. MOSFET used in various electrical and electronic projects which are designed by using various electrical and electronic components.

CMOS

CMOS uses two complementary MOSFETs, in which one conducts and the other shuts off. The CMOS inverter is a basic digital circuit, CMOS device have the advantage of very low power consumption.

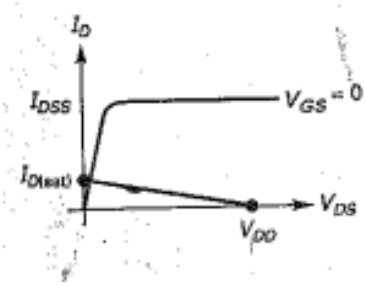
Definitions

Ohmic resistance at pinchoff



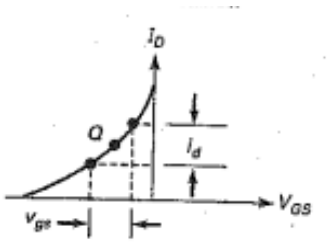
$R_{DS} = V_P / I_{DSS}$

Hard Saturation



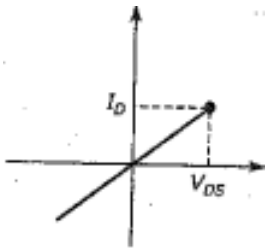
$I_{D(sat)} << I_{DSS}$

Transconductance



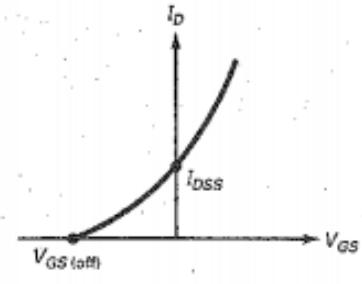
$g_m = i_d / V_{GS}$

Ohmic resistance near origin



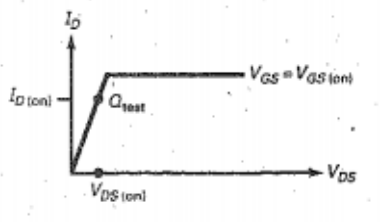
$r_{ds} = V_{DS} / i_D$

D-MOSFET drain current



$I_D = I_{DSS}(1 - V_{GS} / V_{GS(off)})^2$

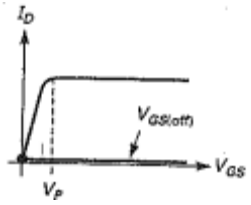
On resistance



$R_{DS(on)} = V_{DS(on)} / I_{D(on)}$

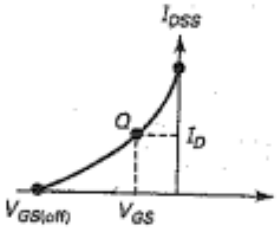
Derivations :

Gate-source cutoff voltage :



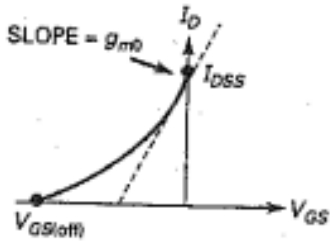
$V_{GS(off)}= -V_P$

Drain current



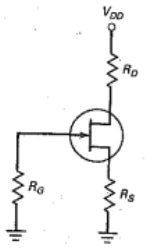
$I_D=I_{DSS}(1-V_{GS}/V_{GS(off)})$

Gate cutoff voltage



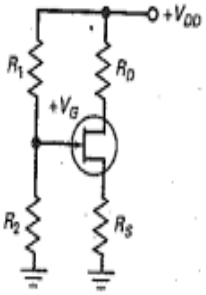
$V_{GS(off)}= -2I_{DSS}/g_{m0}$

Self bias



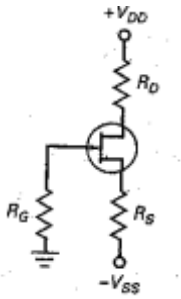
$V_{GS}= -I_DR_S$

Voltage divider bias



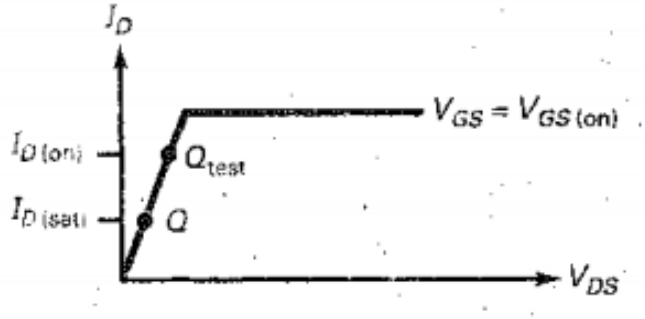
$I_D= (V_G-V_{GS})/R_S \approx V_G /R_S$

Source bias



$I_D = (V_{SS}-V_{GS})/R_S \approx V_{SS} /R_S$

Ohmic region



$I_{D(sat)}< I_{D(on)}$

Long & Short Questions

Q.1. Explain with proper diagram the construction and working of an n-channel JFET. Draw and explain necessary circuit diagram to obtain its characteristics. [Kanpur 2015]

Or

With the help of neat sketches and characteristics curve explain the junction FET. [Important]

Or

What are the different types of field effect transistor ? Draw drain and output characteristics of a field effect transistor . [Important]

Or

Explain pinch-off voltage and draw drain characteristics of FET and also show the parameters of FET and relation between them. [Important]

Related Short Answer Questions

(i)	Write short note on field effect transistor	[Kanpur 2016]
(ii)	Define the characteristic parameters of a FET and establish the relation between them	[Kanpur 2013]
(iii)	Explain the construction of FET	[Important]
(iv)	Describe the construction of an N-channel JFET	[Important]

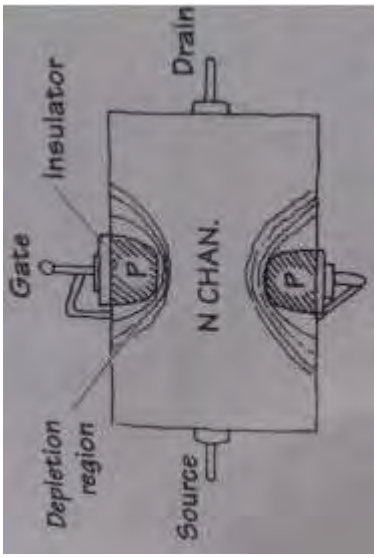
JFET is produced by diffusing two areas of p-type semiconductor into the n-type semiconductor (or two areas of n-type semiconductor into the p-type semiconductor produces p-type JFET) These p- regions are internally connected to get a single external gate lead, the JFET so produced is known as n-channel JFET.

Construction

A N- Channel JFET is a JFET whose channel is composed of primarily electrons as the charge carrier. This means that when the transistor is turned on, it is primarily the movement of electrons which constitutes the current flow.

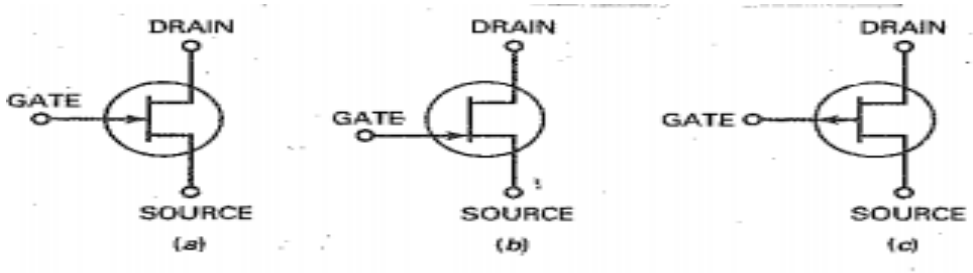
This is in contrast to p-channel JFETs, whose channel is composed primarily of holes, which constitute the current flow.

- A N-Channel JFET is composed of a gate, a source and a drain terminal .It is made with an N-type silicon type silicon channel that contains two P-type silicon terminals placed on either side.
- The gate lead is connected to the p-type terminals, while the drain and source leads are connected to either ends of the N-type channel.



Symbols

Fig.(a) shows schematic symbol of n-channel JFET , fig.(b) shows offset-gate symbol & fig.(c) shows p-channel JFET



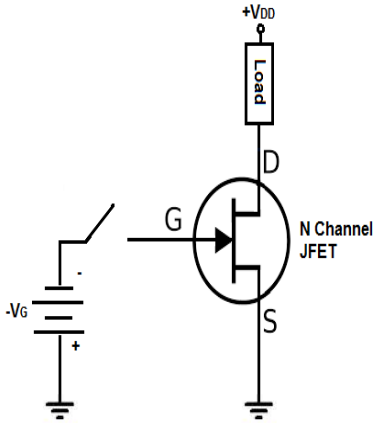
Working

When no voltage is applied to the gate of a N-Channel JFET, current flows freely through the central N-channel. This is why JFETs are referred to as "normally on" devices. Without any applied to the gate terminal of the transistor, they conduct current across from drain-source region.

Typical diagram of voltage biasing of a N- channel JFET is shown in the figure.

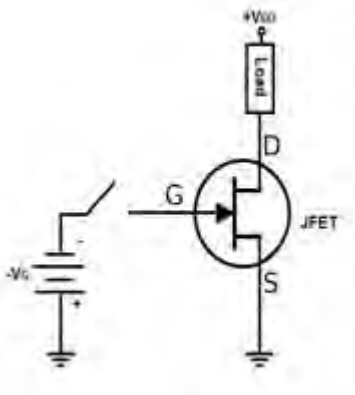
To turn on an N-JFET , + V_{DD} is applied to the drain terminal of the transistor with no voltage applied to the gate terminal of the transistor. This will allow a current to flow through the drain-source channel. If the gate voltage, V_G, is 0V, the drain current is at its largest value for safe operation, and the JFET is in the ON active region.

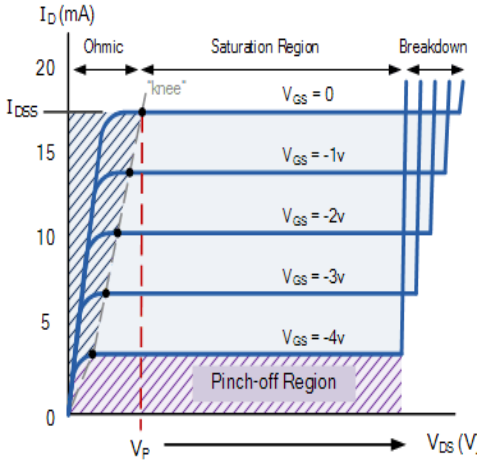
So with a sufficient positive voltage, VDD, and no voltage (0V) applied to the base, the N-channel JFET is in maximum operation and has the largest current.



Voltage biasing of N-channel JFET

Characteristics curve





The voltage V_{GS} applied to the gate controls the current flowing between the drain and the source terminals. V_{GS} refers to the voltage applied between the gate and the source while V_{DS} refers to the voltage applied between the drain and the source.

The characteristics curves shown above, shows the four different regions of operation for a JFET and these are given as:

Ohmic Region : When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

Cut-off Region : This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.

Saturation or Active Region : The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.

Breakdown Region : The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current

Q.2. Describe the action of JFET as a switch in electronic circuits. [Important]

When JFET acts as a switch it either transmits or blocks a small signal ac signal. To get this type of action, the gate-source voltage V_{GS} has only two values : either zero or a value that is greater than $V_{GS(off)}$. In this way JFET operates either in the ohmic region or in the cutoff region.

Shunt Switch

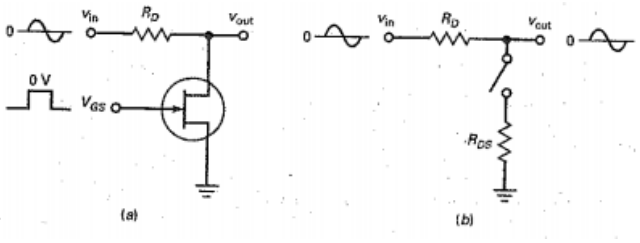


Fig.(a) shows a JFET shunt switch. The JFET is conducting or cut off, depending on whether V_{GS} is high or low.

When V_{GS} is high(0V), the JFET operates in the ohmic region & when V_{GS} is low, the JFET operates in the cutoff as shown in fig.(b).

For normal operation , the ac input voltage must be a small signal, that ensures that the JFET remains in the ohmic region when the ac signal reaches its positive peak. Also R_D is much grater then R_{DS} to ensure hard saturation

$$R_D >> R_{DS}$$

When V_{GS} is high , JFET operates in the ohmic region & the switch is closed therefore $V_{out} = 0V$, when V_{GS} is low, the JFET operates in the cutoff region , so the switch is open. In this case $V_{out} \approx V_{in}$ Therefore , the JFET shunt switch either transmits the ac signal or blocks it.

Series switch

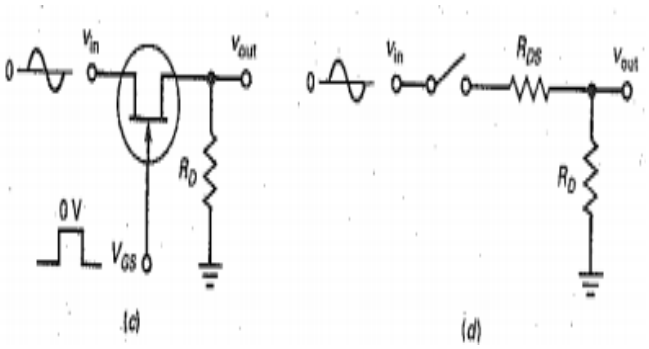
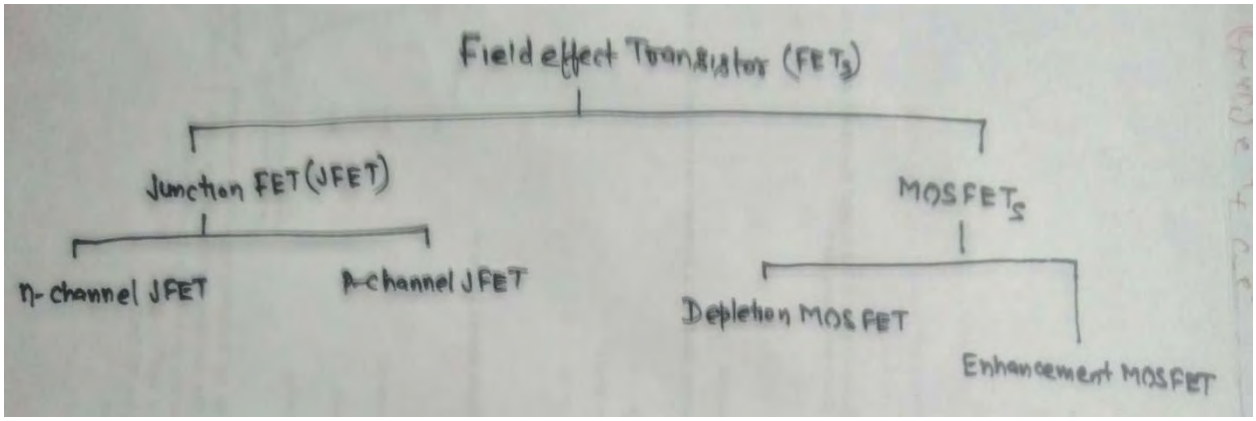


Fig.(c) shows JFET series switch & fig.(d) is equivalent to a resistance of R_{DS}. In this case, the output is approximately equals to input.

When V_{GS} is low , the JFET is open and v_{out} is approximately zero.

When V_{GS} is high i.e. zero , the JFET is close and $V_{out} \approx V_{in}$

Q.3. Explain the classification of Field effect transistor



Q.4. What is the major difference between unipolar & bipolar device?

The basic difference between unipolar & bipolar devices are as below:-

- FET is unipolar device, means the current flowing through it is only due to one type of charge carriers , holes or electrons. BJT on other hand is a bipolar device as holes & electrons both contribute to the flow of current.
- As there is npn & pnp bipolar transistor, there are n-channel & p-channel field effect transistor.
- FET has very high input impedance of megaohms range, which is much higher than the input impedance of BJT.
- FETs are more temperature stable as compare to the BJT and it requires less space than that for a BJT. Therefore FETs are preferred in Integrated circuits.

Q.5. What is MOSFET ? Bring out the difference between MOSFET's and FET's and BJT's.

[Important]

Related Short Answer Questions

(i) Compare FET with the conventional junction transistor [Kanpur 2016]

(ii) What is difference between FET & bipolar transistor ? [Important]

Comparison between FET and Junction Transistor

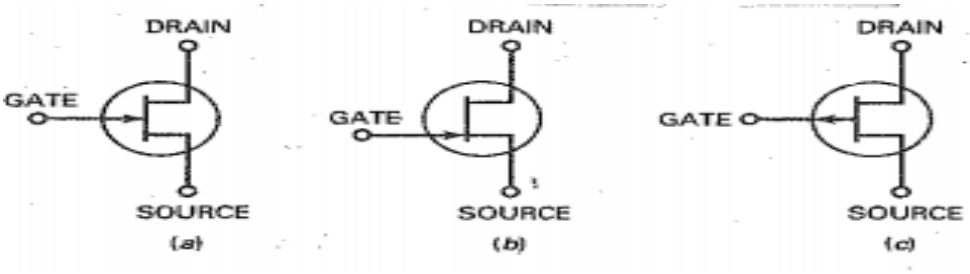
Refer to Q.4.

Comparison between JFET and MOSFET

S.No.	Characteristics	JFET	MOSFET
1	Input Resistance (Ω)	$< 10^9$	$< 10^{12}$
2	Mode of operation	Depletion Mode	Both depletion & Enhancement modes
3	Drain resistance	Higher	Smaller
4	Leakage current	Nearly 10^{-9} A	Nearly 10^{-12} A
5	Output impedance	50kΩ to 1 MΩ	10 kΩ to 50 kΩ
6	Transconductance	1 to 10mAV^{-1}	1 to 10mAV^{-1}

Comparison between NMOS & PMOS

Fig.(a) shows schematic symbol of n-channel JFET , fig.(b) shows offset-gate symbol & fig.(c) shows p-channel JFET



- P-channel is much easier and cheaper to produce compare to N-channel MOSFET device.
- The N-channel MOSFET has high packing density. This makes it faster for switching applications due to smaller junction areas and low inherent capacitances.
- N-channel MOSFET is smaller for same complexity compare to P-channel MOSFET.
- Drain resistance of P-channel MOSFET is 3 times higher than identical N-channel MOSFET device.
- N-channel MOSFET has high false turn-on possibility compare to P-channel device. This is due to positively charged contaminants.
- For given drain current rating, P-channel MOSFET occupies larger area compare to N-channel MOSFET. This is due to the fact that electron mobility is 2.5 times than mobility of hole.

Q.6. What is MOSFET ? Describe the operation of a MOSFET and its types with the help of diagram.

Related Short Answer Questions

(i) Write note on the construction and working of MOSFET. [Kanpur 2015]

(ii) Why are N-channel MOSFET preferred over P-channel MOSFET [Kanpur 2013]

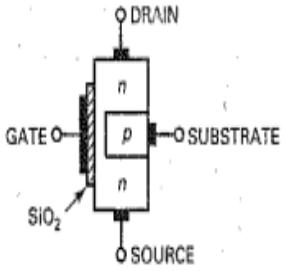
(iii) What do you mean by Enhancement mode of MOSFET [Important]

(iv) Explain the representation and working of a depletion mode of a MOSFET. [Important]

MOSFET is the metal- oxide semiconductor FET, has a source, gate, and drain. The MOSFET differs from JFET, as in MOSFET gate is insulated from the channel due which gate current is smaller than it is in JFET, that is why MOSFET is also known as IGFET which stands for insulated gate FET .

- There are two kinds of MOSFETs, the depletion- mode typeand the enhancement mode type.
- The enhancement mode MOSFET is widely used in both discrete and integrated circuits. In discrete circuits, the main use is in the power switching, which means turning large currents on and off.
- D-MOSFET are used in high-frequency front-end communication circuits as RF amplifier.

The Depletion –Mode MOSFET



Depletion –Mode MOSFET as shown in figure, a piece of n material with insulated gate on the left and a p region on the right. The p region is called the substrate . Electrons flowing from source to drain must pass through the narrow channel between the gate and the p substrate.

A thin layer of silicon dioxide is deposited on the left side of the channel. In a MOSFET the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when gate voltage is +ve.

Fig. (a) shows a depletion-mode MOSFET with a –ve gate voltage. The V_{DD} supply force free electrons to flow through the narrow channel on the left of the p substrate. As with a JFET , the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller is the drain current. When a gate voltage is negative enough , the drain current cutoff.

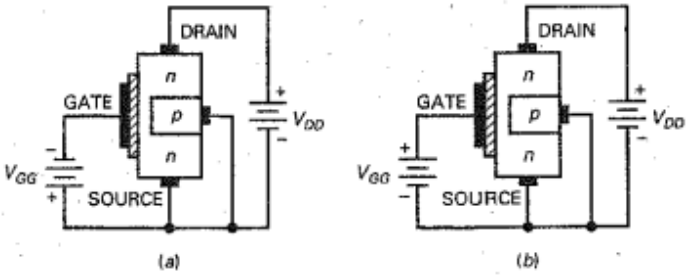
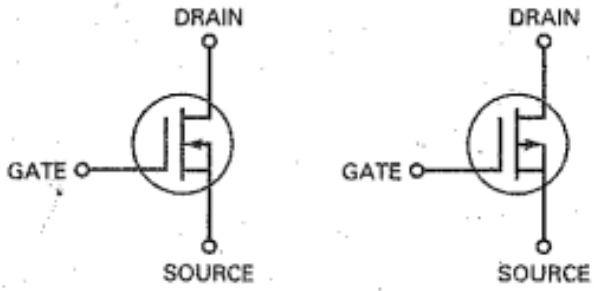


Fig. (b) shows a depletion-mode MOSFET with a + ve gate voltage. The +ve gate voltage increases the number of free electrons flowing through the channel. The more positive the gate voltage, the greater is the conduction from source to drain.

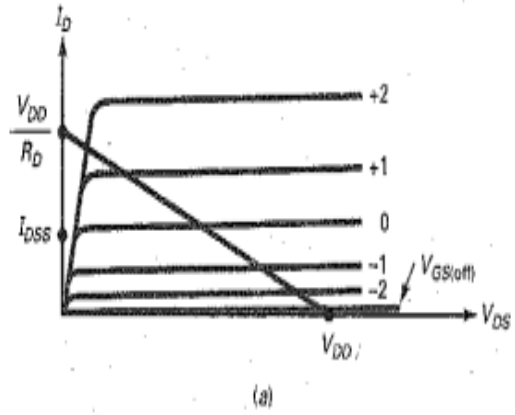
Symbols



n-channel p-channel

D-MOSFET Curves

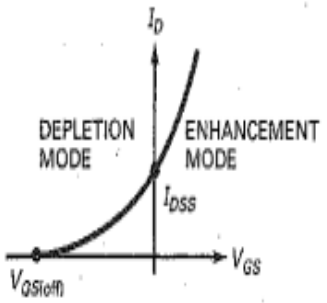
- Fig. (a) shows the set of drain curves for a typical n-channel, depletion –mode MOSFET. The curves above V_{GS}= 0 are positive and the curves below V_{GS}= 0 are negative.
- The bottom curve is for $V_{GS(off)}$ and the drain current will be approximately zero.
- When V_{GS}= 0 , the drain current will be I_{DSS}. This shows that D-MOSFET is a normally on device.
- When V_{GS}< 0 , the drain current is reduced
- When V_{GS} is +ve , I_D will increase following the square-law equation.



(a)

$$I_D=I_{DSS}(1- V_{GS}/ V_{GS(off)})^2$$

- When VG<0 i.e. –ve , the D-MOSFET is operating in the depletion mode. When V_{GS} is +ve , the D-MOSFET is operating in the enhancement mode. Like the JFET, the D-MOSFET curves display an ohmic region, a current source region and a cutoff region.
- Fig.(b) is the transconductance curve for D-MOSFET. I_{DSS} is the drain current with gate shorted to the source.
- The parabolic curve follows the same square-law relation that exits with JFET



(b)

Q.7. Explain the basic operation & output characteristics of n-channel depletion type MOSFET. [Important]

Refer to Q.6.

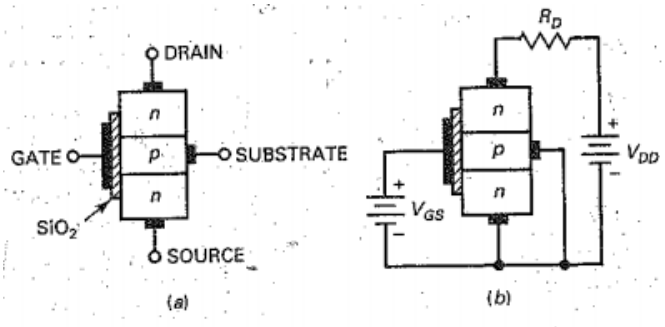
Q.8. Explain with proper diagram, the construction and working of a n-channel e- MOSFET. Draw and explain necessary circuit diagram to obtain it characteristics . [Kanpur 2014]

Or

What is enhancement MOSFET ? What do you understand by threshold voltage . [Important]

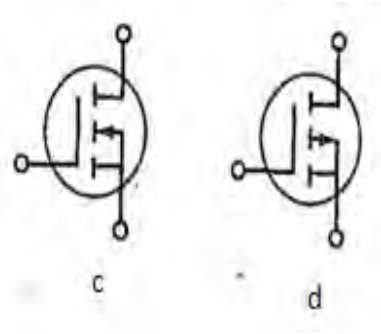
The E-MOSFET as shown in figure(a). The p substrate now extends all the way to the silicon dioxide i.e. there is no longer n channel between the source and the drain.

- Fig. (b) shows normal biasing polarity, when the gate voltage is zero, the current between source and drain is zero, for this reason , an



E-MOSFET is normally off when the gate voltage is zero.

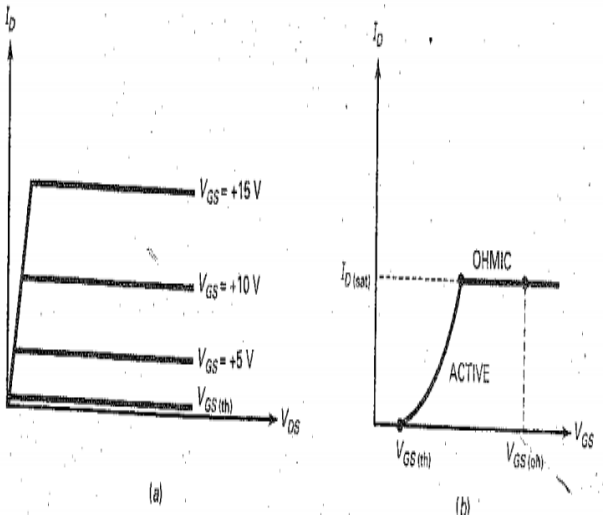
- When the gate voltage is positive, it attracts free electrons into the p region. The free electrons recombines with the holes next to the silicon dioxide.
- When the gate voltage is positive enough, all the holes touching the silicon dioxide are filled and free electrons begin to flow from source to drain.
- The effect is same as creating a thin layer of n-type material next to the silicon dioxide. This thin conducting layer is called the n-type inversion layer. Due to formation of inversion layer electrons can flow easily from the source to the drain.
- The minimum V_{GS} that creates the n-type inversion layer is called the **threshold voltage,** symbolized $V_{GS(th)}$.
- When V_{GS} is less than $V_{GS(th)}$, the drain current is zero. When V_{GS} is greater than $V_{GS(th)}$, an n-type inversion layer connects the source to the drain and the drain current can flow. Typical values of $V_{GS(th)}$ for small-signal devices are from 1 to 3V.
- The schematic symbol is shown in fig. (c) & (d) has a broken channel line indicate this normally off condition.
- The arrow points to inversion layer , which acts like an n channel when the is
- The E-MOSFET is called enhancement because a gate voltage greater than the threshold voltage enhances the conductivity.
- With zero gate voltage, a JFET is on, whereas an E-MOSFET +is off. Therefore, the E-MOSFET is considered to be a normally off device.



Drain Curves

Figure (a) shows a set of drain curves for a typical small-signal E-MOSFET.

- The lowest curve is the $V_{GS(th)}$ curve, when the V_{GS} is lesser then $V_{GS(th)}$, the drain current is approximately zero.
- When the V_{GS} is grater then $V_{GS(th)}$, the device turns on and the drain current is controlled by the gate voltage.
- The almost –vertical part of the graph is the ohmic region, and the almost horizontal part is the active region.
- When biased in the ohmic region , the E-MOSFET is equivalent to a resistor. When biased in the active region , it is equivalent to a current source.



Figure(b) shows a typical transconductance curve .

- There is no drain current until V_{GS}= $V_{GS(th)}$.
- The drain current increases rapidly until it reaches the saturation current $I_{D(Sat)}$.
- Beyond $I_{D(Sat)}$, the device is biased in ohmic region
- No change in I_D , even though V_{GS} increases .
- To ensure hard saturation , a gate voltage $V_{GS(on)} > V_{GS(th)}$.

Q.9. Explain how output characteristics of a MOSFET are obtained . Illustrate with proper electronic circuits. Draw output characteristics of depletion type & enhancement type MOSFET and explain the difference between them. [Important]

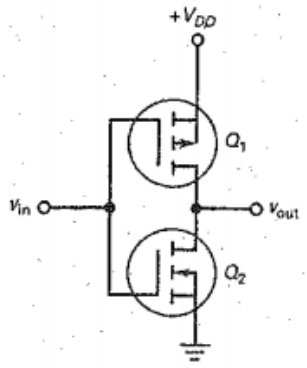
Ref. to Q.6. & Q.8.

Difference between depletion type & enhancement type MOSFET

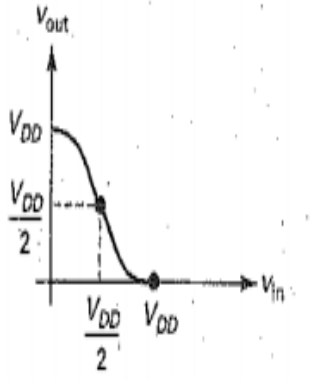
1. Enhancement type mode MOSFET will be off for gate to source voltage 0V as there exists no channel to conduct. Depletion type MOSFET conducts at 0V has positive cut off gate voltage so less preferred. Depletion MOS also conducts at 0V therefore has less useful application.
2. Since the logic operations of depletion MOSFET is the opposite to the enhancement MOSFET, the depletion MOSFET produces positive logic circuits, such as, buffer, AND, and OR.
3. Diffusion current (i.e. sub-threshold leakage current) exists in enhancement MOSFET while depletion MOSFET do not have any diffusion current.
4. As a enhancement MOSFET shrinking in size, there is no way to stop the sub threshold leakage current diffused across from source to drain because the drain and source terminals are closer physically. This is not the problem with depletion type MOSFET because a pinched channel stops the diffusion current completely.
5. Depletion MOSFET logic operations are opposite to enhancement type of MOSFETs.

Q.10. Explain with proper diagram, the construction CMOS. What are the advantages of CMOS over MOSFET ?

CMOS stands for complementary MOSFET as shown in fig. consists of enhancement type n-MOS & p-MOS connected in series with common gate terminal acting as v_{in}.



- The input signal is either $(+V_{DD})$ or (0V). When the input voltage is high Q_1 is OFF & Q_2 is ON.
- In this case , the shorted Q_2 pulls the output voltage down to ground.
- When the input voltage is low Q_1 is ON & Q_2 is OFF.
- In this case , the shorted Q_1 pulls the output voltage up to $+V_{DD}$.
- Since the output voltage is inverted the circuit is called a CMOS inverter.
- For CMOS voltage transfer characteristics i.e. VTC is shown in VTC curve.



VTC curve

Advantages of CMOS

1. Steady state power of CMOS is zero.
2. VTC(voltage transfer characteristics) is nearly ideal i.e. voltage swing is from 0 to V_{DD}.
3. Both NMOS , PMOS acts as load for low and high I/P respectively.
4. Have high FAN IN & FAN OUT.
5. Have high noise margin.

Numerical

Q.1. A JFET has $V_{GS(off)}$ =-4V & I_{DSS}= 5mA. What are the gate voltage & drain current at the half cutoff point ?

Exp: At half cutoff point V_{GS}= -4V/2 = -2V

$\because I_D = I_{DSS}(1- V_{GS}/ V_{GS(off)})^2$

$\therefore I_D = 5mA(1-2/4)^2$

$= 5mA/4 = 1.25mA$ Ans

Q.2. A JFET has I_{DSS}= 5mA and g_{m0}= 500µS. What is the value of $V_{GS(off)}$? What does g_m equal when V_{GS} = -1V ?

Exp: $\because g_{m0} = -2\ I_{DSS}/ V_{GS(off)}$

$\therefore V_{GS(off)} = -2\ I_{DSS}/ g_{m0}$

$\therefore V_{GS(off)} = -2(5mA)/ 500\mu S = -2V$

$\because g_m = g_{m0}\ (1- V_{GS}/ V_{GS(off)})$

$\therefore g_m = (500\ \mu S)\ (1- 1/2)$

$= 2500\ \mu S$ Ans

Q.3. The following readings were obtained in an experiment with FET.

V_{GS}(Volts)	V_{DS}(Volts)	I_D(mA)
0.0	**06**	**12**
0.0	**16**	**12.3**
0.3	**16**	**12.0**

Calculate

(i) AC drain resistance (ii) Transconductance (iii) Amplification Factor [Important]

Exp: According to the given reading

For constant V_{GS} at 0V

(i) Change in drain to source voltage (ΔV_{DS}) = 16-6 = 10V

Change in drain Current (ΔI_D) = 12.3-12 = 0.3mA

$\because$ AC drain resistance(r_d) = ΔV_{DS} / ΔI_D at constant V_{GS}

$\therefore r_d = 10V/0.3mA = 33.3k\Omega$

(ii) Drain current changes from 12.3mA to 12mA and V_{GS} changes from 0.0V to 0.3V at constant V_{DS} that is at 16V.

ΔV_{GS}= 0.3- 0.0 = 0.3V

ΔI_D = 12.3-12 = 0.3mA

$\because$ Transconductance(g_m) = ΔI_D / ΔV_{GS} at constant V_{DS}

$\therefore g_m = 0.3mA / 0.3V = 0.3m$ mho

(iii) Amplification Factor (μ) = $r_d . g_m$

$\therefore \mu = 33.3k\Omega$ x 0.3m mho = 33.3 Ans

Q.2. The following readings were obtained in an experiment with FET.

V_{GS}(Volts)	V_{DS}(Volts)	I_D(mA)
0.0	**7**	**10**
0.0	**15**	**10.25**
-0.2	**15**	**9.65**

Calculate

(i) AC drain resistance (ii) Transconductance

(iii) Amplification Factor of JFET

[Important]

Exp: According to the given reading

For constant V_{GS} at 0V

(i) Change in drain to source voltage (ΔV_{DS}) = 15-7 = 8V

Change in drain Current (ΔI_D) = 10.25-10 = 0.25mA

$\because$ AC drain resistance(r_d) $= \Delta V_{DS} / \Delta I_D$ at constant V_{GS}

$\therefore r_d = 8V/0.25mA = 32k\Omega$

(ii) Drain current changes from 10.25mA to 9.65mA and V_{GS} changes from 0.0V to -0.2 at constant V_{DS} that is at 15V.

ΔV_{GS}= -0.2- 0.0 = -0.2V

ΔI_D = 9.65-10.25 = -0.6mA

$\because$ Transconductance(g_m) $= \Delta I_D / \Delta V_{GS}$ at constant V_{DS}

$\therefore g_m = -0.6mA / -0.2V = 0.3m$ mho

(iii) Amplification Factor (μ) = $r_d . g_m$

$\therefore \mu = 32k\Omega \times 0.3m$ mho $= 96$ Ans

Q.3. When V_{GS} of a FET changes from -3.1V to -3V the drain current changes from 1mA to 1.3mA. What is the value of transconductance ? [Important]

Exp: Given ΔV_{GS}= (-3V)-(-3.1V)= 0.1V

ΔI_D = 1.3mA - 1mA= 0.3mA

$g_m = ?$

$\because$ Transconductance(g_m) $= \Delta I_D / \Delta V_{GS}$

$\therefore g_m = 0.3mA / 0.1V = 3m$ mho Ans

Q.4. When gate- source voltage V_{DS} of a FET changes from -3.1V to -2.9V the drain current changes from 1mA to 1.2mA. What is the value of transconductance ? [Kanpur 2013]

Exp: Given ΔV_{GS}= (-2.9V)-(-3.1V)= 0.2V

ΔI_D = 1.2mA - 1mA= 0.2mA

$g_m = ?$

$\because$ Transconductance(g_m) $= \Delta I_D / \Delta V_{GS}$

$\therefore g_m = 0.2mA / 0.2V = 1m$ mho Ans

Q.5. An n-channel FET has I_{DSS} =12mA and pinch off voltage V_P = -4V . Find drain current for V_{GS} = -2V , where symbols have their usual meanings. [Kanpur 2012]

Exp: Given I_{DSS} =12mA, V_P = -4V, V_{GS} = -2V , I_D = ?

$\because I_D = I_{DSS}(1 - V_{GS} / V_{GS(off)})^2$

$\therefore I_D = 12mA(1-2/4)^2 = 6mA$ Ans

Q.6. An n-channel silicon JFET has a donor concentration of 2x 10^{21}/ m^3 and a channel width of 4µm , If the dielectric constant of silicon is 12, find the pinch off voltage. [Kanpur 2015]

Exp: Given N_D = 2x 10^{21}/ m^3 , Channel width= 4 x10^{-6}m , $k_{silicon}$= 12

V_P(pinch off voltage) =?

$\because V_P = \frac{e N_D}{2\epsilon} a^2$,

Putting the values from given data , we have

$\therefore V_P = \frac{e N_D}{2k\epsilon_0} a^2$

$\therefore V_P$ = [1.6x 10^{-19} x 2x 10^{21}] x4 x10^{-6}/ [2x 12 x 8.86 x 10^{-12}]

= 6.02volt Ans

Q.7. Sketch the transfer characteristics for an n-channel depletion-type MOSFET with I_{DSS} =10 mA and V_P =-4V.

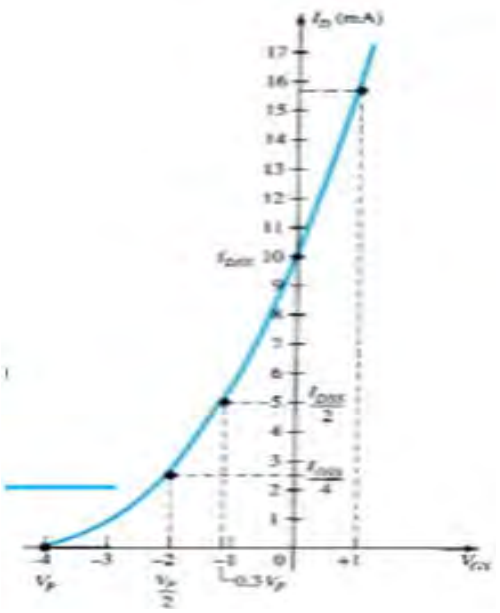
Exp: At V_{GS}= 0V , I_D= I_{DSS}= 10mA

V_{GS}= V_P = -4V , I_D= 0mA

V_{GS}= V_P /2= -4V /2 = -2V , I_D= 10mA(1-2/4)^2 =2.5mA

At I_D= I_{DSS}/2 , We have V_{GS}= 0.3V_P = -1.2V

Plotting all these points we have transfer characteristics as shown in figure.



Chapter-8
Power Supplies

The Half- Wave Rectifier

The half wave rectifier has a diode in series with a load resistance. The load voltage is a half- wave output. The average or dc voltage out of a half-wave rectifier equals 31.8 percentage of the peak voltage.

The Transformer

The input transformer is usually a step-down transformer in which the voltage steps down and the current step up. The secondary voltage equals the primary voltage divided by the turn ratio.

Filters

Filters are circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal, to enhance wanted ones, or both.

Passive Filters

Filters that are based on combinations of resistors (R), inductors (L) and capacitors (C), known as *passive filters*, these filters do not depend upon an external power supply and/or they do not contain active components such as transistors.

Active Filters

Active filters are implemented using a combination of passive and active (amplifying) components, and require an outside power source. Operational amplifiers are frequently used in active filter designs.

Filter Responses

There are five basic types of responses : low-pass, bandpass, bandstop and all-pass. The first four have a pass-band and a stop-band. Ideally, the attenuation band zero in the pass-band and infinite in the stop-band.

Approximate Responses

The pass-band is identified by its low attenuation and its edge frequency. The stop-band is identified by its high attenuation and edge frequency. The order of the filter is the number of reactive components. With active filters, it is usually the number of capacitors .

First-Order Stages

First-order stages have a single capacitor and one or more resistor. All first –order stages produce a butterworth response because peaking is possible only in second-order stages.

Higher-Order Filters

Higher-order filters are usually made by cascading first order filter . When filters are cascaded , we add the decibel gain.

Supply Characteristics

Load regulation indicates how much the output voltage changes when the load current changes. Line regulation indicates how much the load voltage changes when the line voltage changes. The output resistance of load determines the load regulation.

Shunt Regulators

The zener regulator is the simplest example of a shunt regulator. By adding transistors and an op-amp, we can build a shunt regulator that has excellent line & load regulation. The main disadvantage of shunt regulator is its low efficiency, caused by power losses in the series resistor and shunt transistor.

Series Regulators

By using a pass transistor instead of a series resistor, we can build series regulator with higher efficiency then shunt regulator. The zener follower is the simplest example of a series regulator. By adding transistors and op amp, we can build series regulators with excellent line and load regulation, plus current limiting.

Power supply

The combination of a transformer ,a rectifier and a filter constitutes an ordinary dc power supply also known as unregulated power supply.

Regulated power supply

A regulated power supply is an electronic circuit designed to provide constant dc voltage of predefined value across load terminals, which is independent of variations in load current, ac mains voltage & temperature.

Voltage regulator

A Voltage regulator is a circuit that supplies a constant voltage regardless of variations in load current and in ac mains voltage.

Switching Regulators

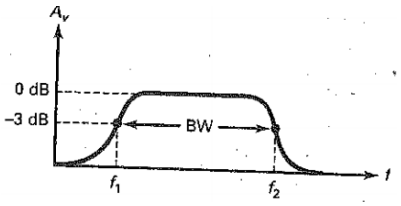
A switching regulator is a dc-to-dc converter that uses pulse-width modulation to regulate the output voltage.

Uninterruptable power supplies (UPS)

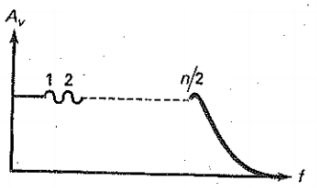
An UPS is just an alternative source that consists of a rectifier, battery charger , a battery bank and inverter circuit which converts the commercial ac input into dc suitable for input to the battery bank and the inverter.

Definitions

Bandwidth

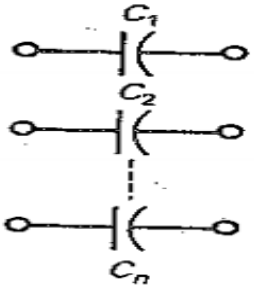


Number of ripples :

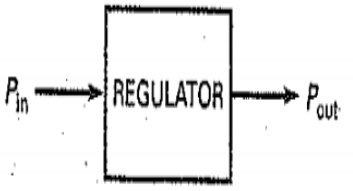


#Ripples = n/2

Efficiency



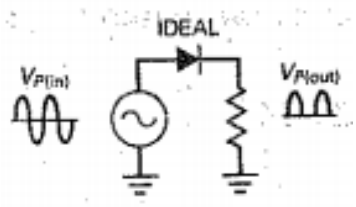
n= # capacitors



Efficiency= P_{out} / P_{in} x 100 %

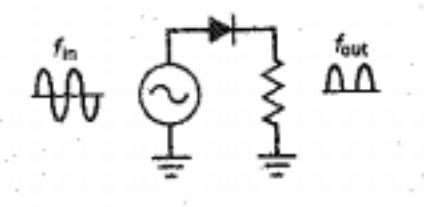
Derivations

Ideal half- wave

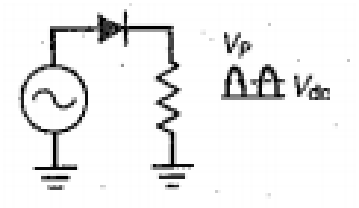


$V_{P(out)} = V_{p(in)}$

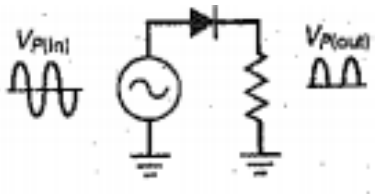
Half-wave



$V_{dc}= V_p/\pi$



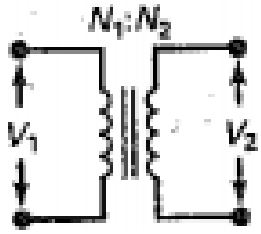
$f_{out}=f_{in}$



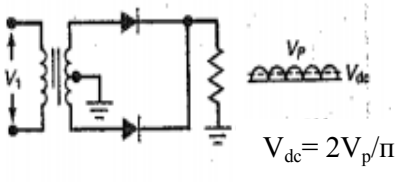
$V_{p(out)}= V_{P(in)}- 0.7V$

Ideal Transformer

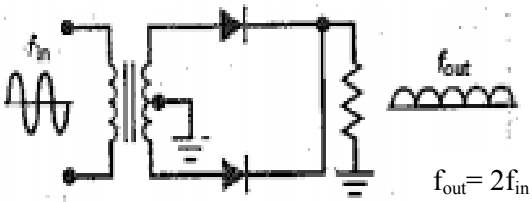
$V_2= V_1/[N_1/ N_2]$



Full Wave



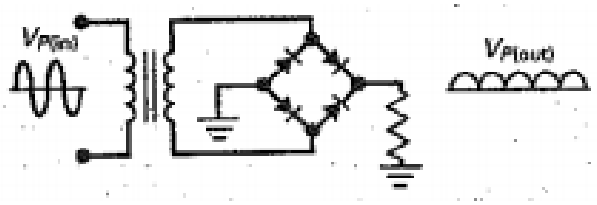
$V_{dc}= 2V_p/\pi$



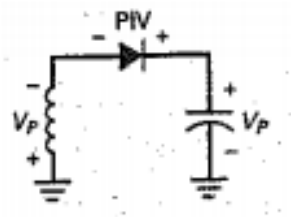
$f_{out}= 2f_{in}$

Bridge rectifier

$V_{p(out)}= V_{p(in)}$ -1.4V

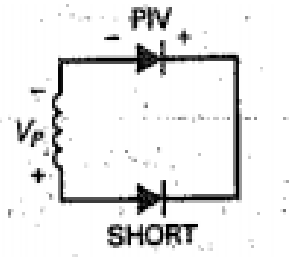


Half wave PIV



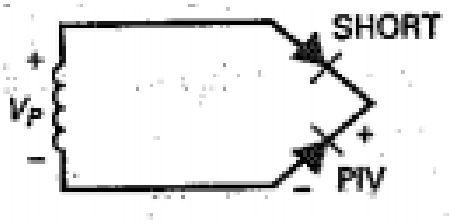
PIV= $2V_P$

Full wave PIV

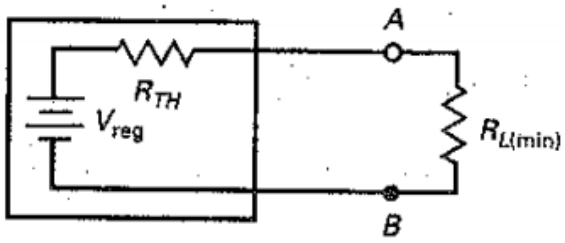


PIV= V_P

Bridge PIV



Load regulation

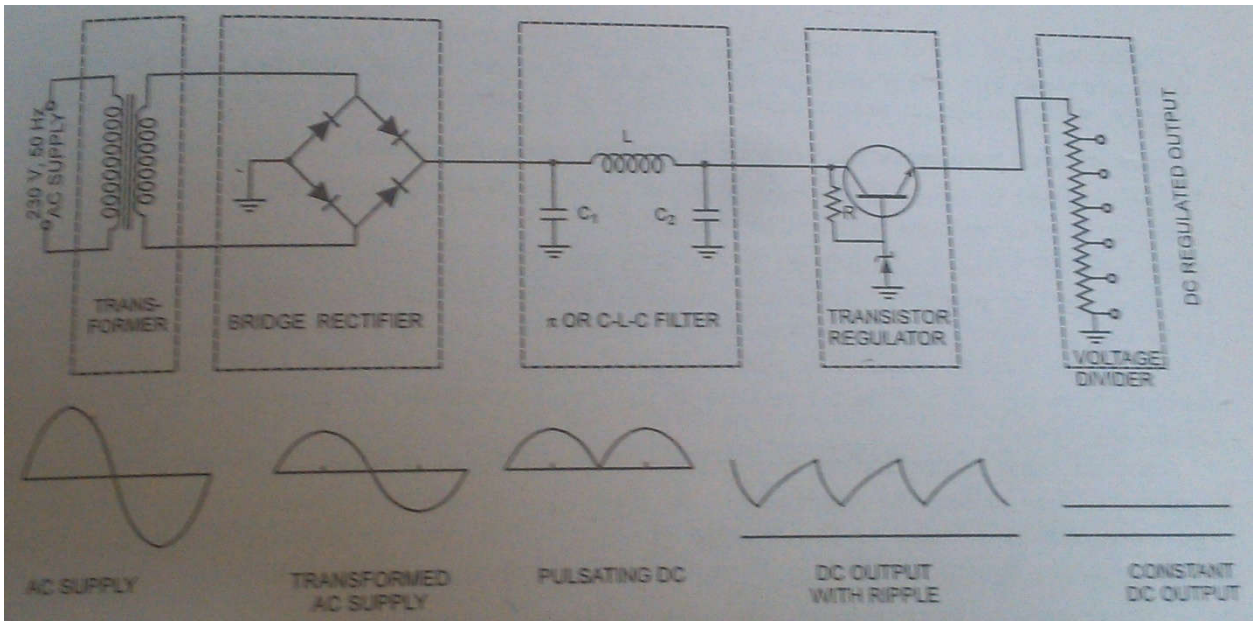


Load regulation = $\frac{R_{TH}}{R_{L(min)}} x\ 100\ \%$

Long & Short Questions

Q.1. What is power supply ? Explain its working . [Kanpur 2012]

The combination of a transformer ,a rectifier and a filter constitutes an ordinary dc power supply also known as unregulated power supply.
A regulated power supply is an electronic circuit that is designed to provide a constant dc voltage of predefined value across load terminals irrespective of ac mains fluctuations or load variations. Fig. shows the complete circuit of a regulated power supply with a transistor series regulator as a regulating device .



- The ac voltage , typically $230V_{rms}$ is connected to a transformer which transforms that ac voltage to the level for desired dc output .
- A bridge rectifier then provides a fullwave rectified voltage that is initially filtered by a pi filter or C-L-C filter to produce a dc voltage. The resulting dc voltage usually has some ripple or ac voltage variation.
- A regulating circuit use this dc input to provide a ripple free dc voltage . The regulated power supply is available across a voltage divider.
- Often more than one dc voltage is required for the operation of electronic circuits. A single power supply can provide as many as voltages as are required by using a voltage divider as shown in the figure.
  A potential divider is a single tapped resistor connected across the output terminals of the supply.

Power Supply Characteristics

The quality of power supply depends on different factors such its load voltage, load current, voltage regulation, source regulation, output impedance, ripple rejection etc. Some of the characteristics of regulated power are discussed below.

1. **Load Regulation:** The load regulation , abbreviated as LR (also called the load effect), is the change in regulated output voltage when the load current changes from minimum to maximum value i.e.

$$LR = V_{NL} - V_{FL}$$

Where V_{NL} is load voltage at no load and V_{FL} is the load voltage at full load.

2. **Minimum Load Resistance:** The load resistance at which a power supply delivers its full-load rated current at rated voltage is referred to a minimum load resistance, $R_{L(min)}$.

i.e. $R_{L(min)} = V_{FL} / I_{FL}$

3. **Source or line Regulation :** Defined as the change in regulated output voltage for a specified range of line voltage, typically 230V± 10 % .

$$\%SR = \frac{(V_{NL} - V_{FL})}{Normalized\ load\ voltage} X\ 100$$

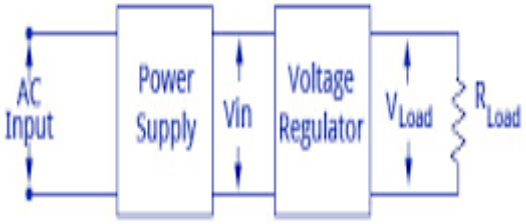
3. **Output Impedance :** A regulated power supply is a very stiff dc voltage source. This means that the output resistance is very small (in milliohms). Even though the external load resistance is varied , almost no change is seen in the load voltage. An ideal voltage source has an output impedance of zero.
4. **Ripple rejection :** Voltage regulators stabilize the output voltage against variations in input voltage . Ripple is equivalent to a periodic variation in the input voltage. Thus a voltage regulator attenuates the ripple that comes in with the unregulated input voltage.

Q.2. What do you mean by regulated power supply

Related Short Answer Questions

(i) Write short notes on electronically regulated power supply. [Kanpur 2014]

A **regulated power supply** is an embedded circuit; it converts unregulated AC into a constant DC. With the help of a rectifier it converts AC supply into DC.
Its function is to supply a stable voltage (or less often current), to a circuit or device that must be operated within certain power supply limits. The output from the regulated power supply may be alternating or unidirectional, but is nearly always DC.



Applications

- Mobile Phone power adaptors
- Regulated power supplies in appliances
- Various amplifiers and oscillators
- D.C. variable bench supply (a **bench power supply** usually refers to a power supply capable of supplying a variety of output voltages useful for bench testing electronic circuits, possibly with

continuous variation of the output voltage, or just some preset voltages; a laboratory (lab) power supply normally implies an accurate bench power supply, while a balanced or tracking power supply refers to twin supplies for use when a circuit requires both positive and negative supply rails).

Q.3. Explain the working of a voltage regulated power supply by drawing its circuit diagram .

[Important]

Refer to Q.1

Q.4. Why unregulated power supply is not good enough for many applications in electronics ?

Since the output voltage available from an unregulated power supply varies with the variations in load current, ac mains voltage ,temperature etc , these variations in dc output voltage may cause inaccurate or malfunctioning of many electronic circuits. Unregulated power supply is not considered suitable for many of the applications in electronics.

Q.5. Why are electronic generators in great demand ?

There is acute storage of power in the country and during summer, power cuts of 1 to 4 hours duration are common in cities & villages. Every home dreams of buying a generator during that time and in comparison to kerosene operated generators , the electronic generators, commonly known as inverters, are attractive due to their low cost and enhanced electronic features. If each home in India buys one inverter, one can imagine what the demand for electronic generators would come to.

Q.6. Differentiate between On-line UPS , off line UPS & Electronic Generators

S. No.	On-line UPS	Off- line UPS	Electronic Generator
1.	Inverter is ON all the time and supplies output power switching time ≈ 0ms	Inverter is ON when mains is OFF. switching time <5ms	Inverter is ON only when mains is OFF switching time =30-100ms
2.	Used for mainframe or work-station computers or in applications where an uninterrupted supply is a must.	Used with PCs or computers or other appliances where a power interruption for 5ms or less does not matter, when the mains supply fails.	Used in houses & offices to run fans, lights, TV , VCR, medical equipment, PC where switching time of 100ms does not matter.
3.	Generally sine-wave inverters used	Sine-wave inverters / Square wave inverters with CVT used.	Generally square-wave inverters without CVT used
4.	Cost is highest	Cost is medium	Cost is lowest
5.	High quality sealed maintenance-free batteries used	Sealed maintenance-free batteries or other batteries used	Generally automobile lead-acid batteries used
6.	Running time of the inverters is generally less(10min to 30min)	Running time of the inverters is generally less(10min to 30min)	Running time of the inverters is high (1 to 4 hours)

Q.7. Give the concept of load line. **[Kanpur 2013]**

The load line is defined as a line that contains every possible operating point for the circuit. To understand the concept of dc load line consider the common emitter configuration & the output circuit as shown in fig (a) & fig. (b) resp.

Procedure to obtain the DC load line :

- Refer to the collector circuit of the CE configuration & apply KVL to this circuit, we have $V_{CC} - V_{CE} - I_C R_C = 0$
- Rearranging the equation , We have
  $I_C = V_{CE}(-1/R_E) + V_{CC} / R_C$

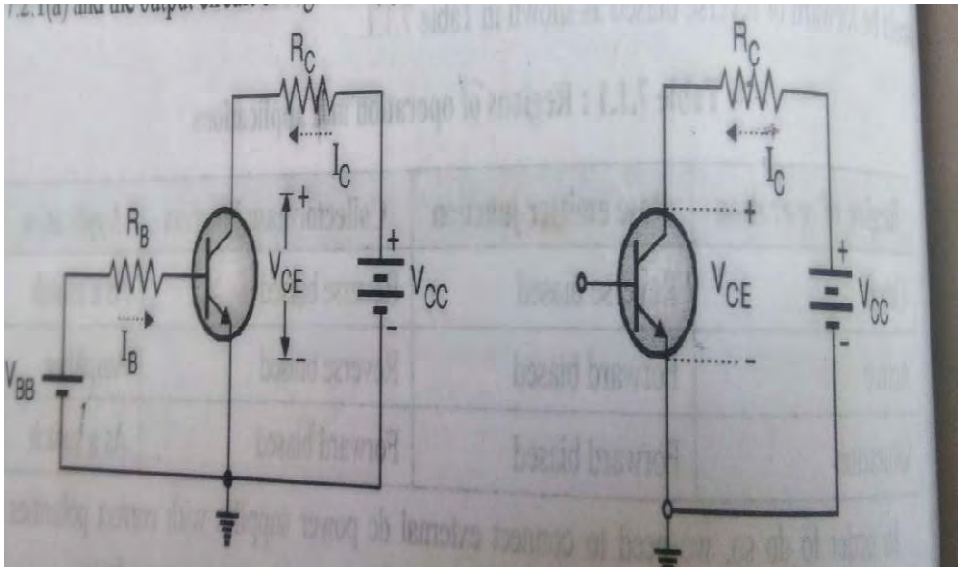


Fig. (a) Fig. (b)

- The above equation is the equation of a straight line ($y = mx + c$) with slope $-1/R_E$ & intercept V_{CC} / R_C.

- This straight line equivalency is known as dc load line.
- DC indicates that this line is drawn under dc operating conditions without ac signal at input

Q.8. What is rectification ? Explain half wave rectifier with diagram. [Important]

Or

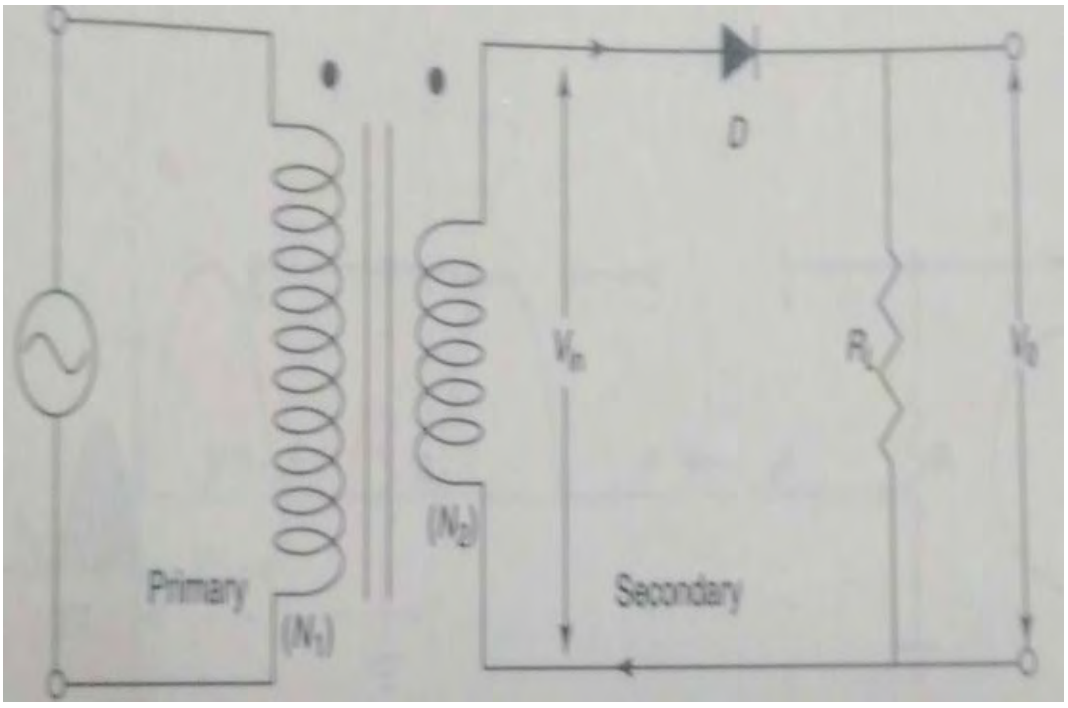
What is rectification ? Draw and explain the diagram of half wave rectifier and explain its working ? How full wave rectifier is better than half wave rectifier ? [Kanpur 2012]

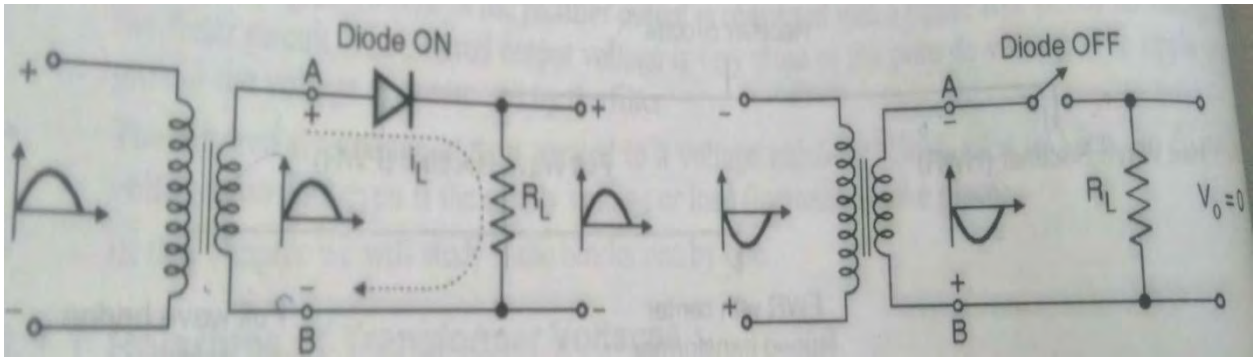
The rectification is a process of converting the alternating waveform to the corresponding direct waveforms. Rectifiers in general, be classified into two categories.

(i) Half- Wave Rectifier
(ii) Full- Wave Rectifier
  a. Centre-tapped transformer full-wave rectifier
  b. Bridge type full-wave rectifier

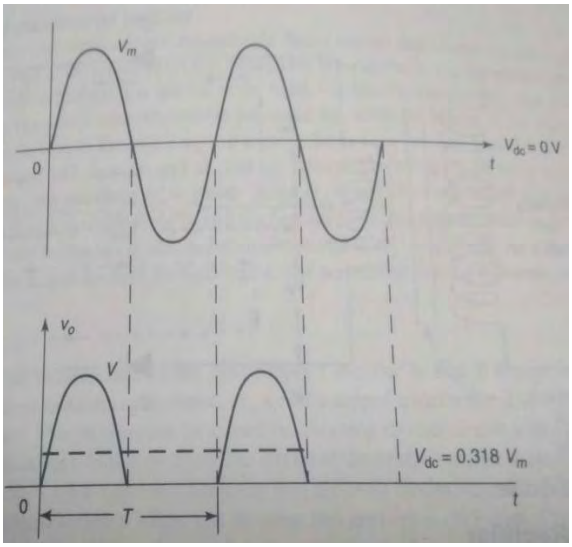
Half –Wave Rectifier

This circuit shown is called as half wave rectifier because it delivers power to the load during only one half cycle of the ac supply voltage.
Hear primary of a transformer is connected to the single phase ac supply , with positive half cycle extends from 0 to T/2 second & the negative half cycle extends from T/2 to T sec.





(a) (b)



In a half-wave rectifier , the output waveform occurs after every alternate half cycle of the input sinusoidal signal.

Between the time interval t = 0 to T/2 , the polarity of the applied voltage v_i is such that makes the diode forward baised (fig. a), as a result output voltage v_0 is obtained between interval t = 0 to T/2.

For the period t = T/2 to T , the polarity of the input voltage is reversed creates reverse baised (fig. b) condition across diode i.e. open circuit state therefore output voltage v_0 is zero for the interval.

The average value of output signal v_0 is 0.318 v_m or v_m/π

The R.M.S. value of output signal is $v_m/2$.

Ripple Factor

The ripple factor indicates how close the rectified output is to the pure ideal dc voltage waveform.

It is denoted by r

$$\text{Ripple factor} = \frac{RMS\ value\ of\ the\ AC\ component\ of\ output}{Dc\ or\ average\ value\ of\ the\ output}$$

$$\mathbf{r} = \sqrt{\frac{V_{rms}^2}{V_{average}^2} - \mathbf{1}}$$

For half wave r= 1.21

Full wave rectifier is better

(i) In the half- wave rectifier, a single diode exists and the load current flows through it for only the +ve half cycle. On the other hand, in a full- wave rectifier, the current flows throughout the cycles of the input signals.

(ii) Full- Wave rectifiers require a centre-tapped transformer. For a half- wave rectifier, only a simple transformer is required.

(iii) The PIV in a half-wave rectifier is the maximum voltage across the transformer secondary. Whereas, in case of a full wave rectifier, the PIV for each diode is two times the maximum voltage between the centre tap and at the either end of the transformer secondary.

(iv) In a half –wave rectifier, the frequency of the load current is the same as that that of the input signal and it is twice the frequency of the input supply for the full- wave rectifier.

(v) The dc load current and the conversion efficiency for a full- wave rectifier is twice that of a half wave rectifier. Also, the ripple factor of the full-wave rectifier is less than that of the half-wave circuit. This indicates that the performance of the full- wave rectifier is better than the half wave rectifier.

(vi) In a full- wave rectifier, two diode currents flows through the two halves of the centre – tapped transformer secondary in opposite directions, so that there is no magnetization of the core. The transformer losses being smaller, a smaller transformer can be used for a full-wave rectifier.

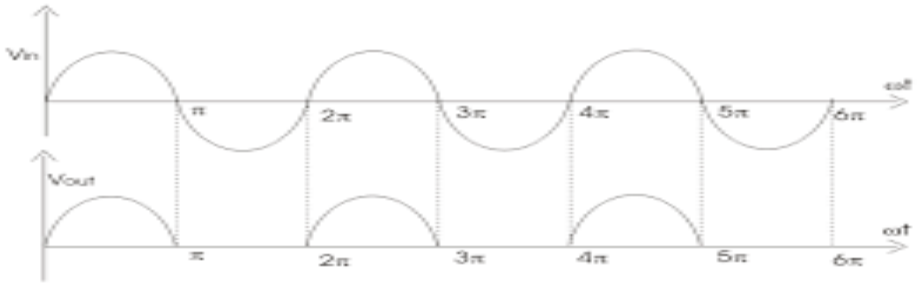
Q.9. Explain the working of half wave rectifier on the basis of energy bands . Derive expressions for average and rms values of output current power efficiency and ripple factor.

[Important]

For working of half wave rectifier refer to Q.8.

Expression for average value

As the load is purely resistive, the average load voltage of a half wave rectifier is



$V_{average} = I_{average} \times R_L$

Average load current (I_{dc})

As load current is available for 0 to π secs & is unavailable for π to 2 π secs with in a complete cycle

Therefore $I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \, sinwt \, dwt = -\frac{I_m}{2\pi}[coswt]_0^{\pi}$,

$I_{dc} = -\frac{I_m}{2\pi}[cos\pi - cos0] = -\frac{I_m}{2\pi}[-1-1] = \frac{I_m}{\pi}$

where I_m = Peak amplitude of the load current with $V_m = peak\ amplitude\ of\ load\ voltage$

Expression for R.M.S. value

Ref. to the waveform in above fig.

$I_{rms} = [\frac{1}{2\pi}\int_0^{\pi} I^2{}_m\ sin^2 wt\ dwt]^{1/2} = [\frac{I^2{}_m}{2\pi}\int_0^{\pi}\frac{1-cos2wt}{2}\ dwt]^{1/2} = \frac{I_m}{2}[\frac{1}{\pi}(\pi - \frac{1}{2}\ sin2\pi)]^{1/2}$,

but $sin2\pi = 0$

Therefore $I_{rms} = \frac{I_m}{2}$

Where, $I_m =\ Peak\ amplitude\ of\ the\ load\ current\ with$

$V_m = peak\ amplitude\ of\ load\ voltage$

Q.10. Explain the working of full wave rectifier drawing its circuit diagram. Derive expression for (i) average and r.m.s. output current (ii) efficiency of rectification (iii) ripple factor of full wave rectifier. [Important]

or

Draw circuit diagram of bridge type full wave rectifier and explain its working. [Important]

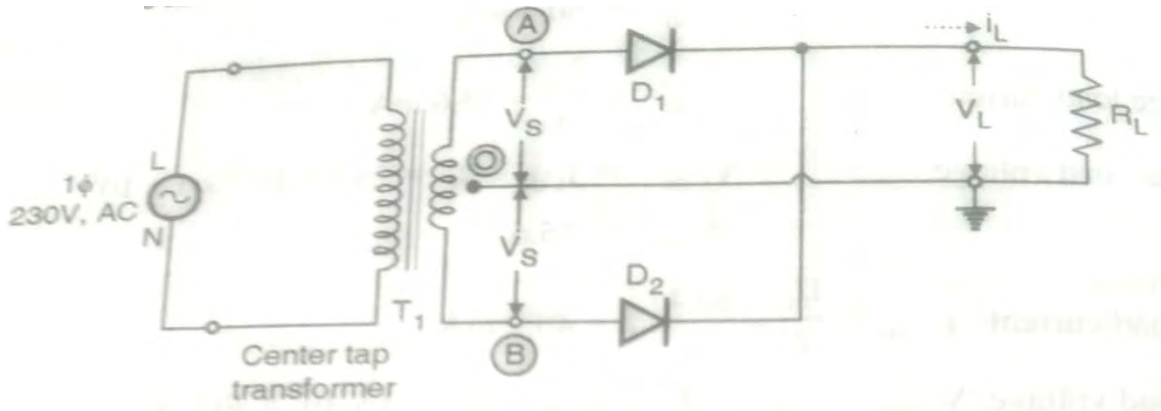
Or

Explain giving circuit diagram the working of a double way rectifier. Why is it widely used ? Obtain expressions for its average and rms values of current and efficiency. What is its main disadvantages. [Important]

Full wave rectifier

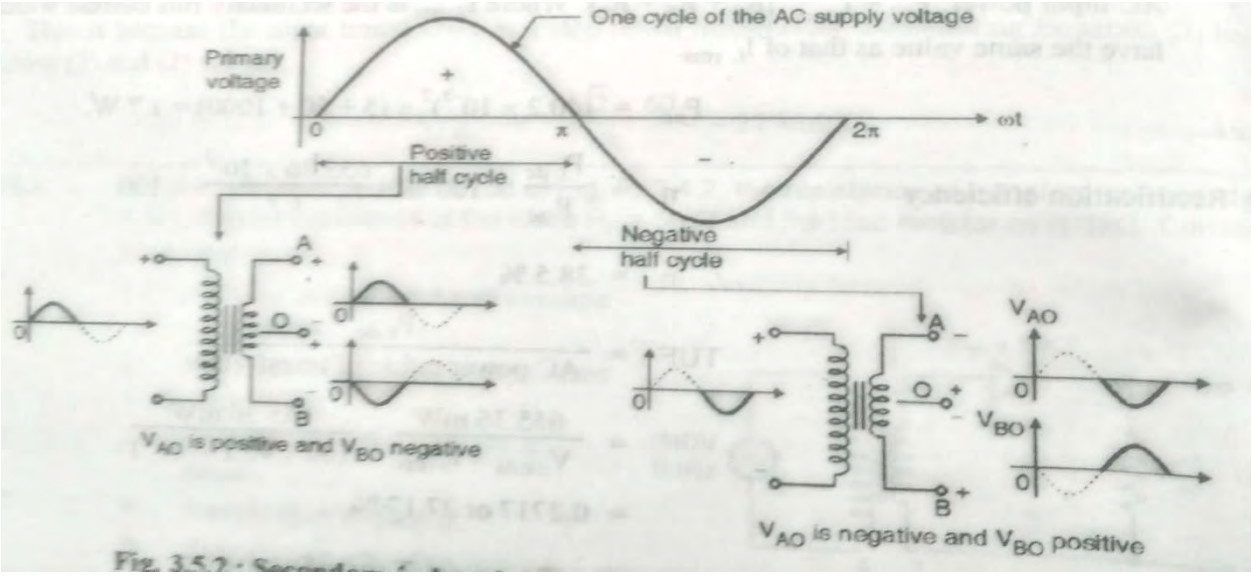
Full wave rectifier configuration is shown in fig. , consists of a step down center taped transformer T_1 , two diodes and a purely resistive load R_L .

In half wave rectifier (HWR) , the load current flows in only one half cycle of the supply but in the full wave rectifier it flows in the both the half cycles of ac supply.



Centre tapped transformer

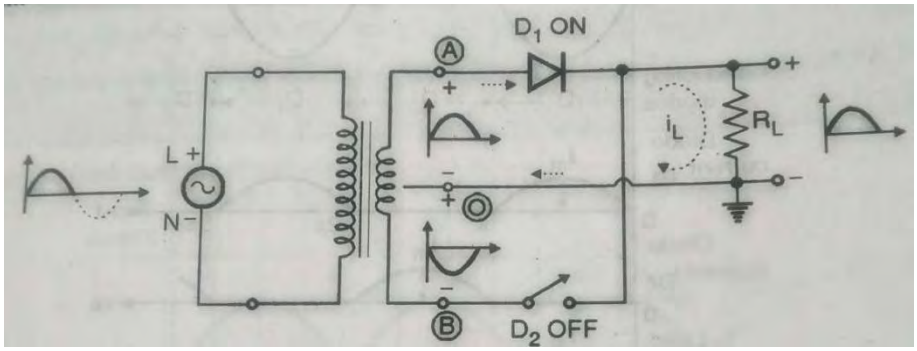
Here, the transformer is of step down type with secondary side centre tapped. The induced voltage in the halves of the secondary winding is always 180^0 out of phase with respect to each other.



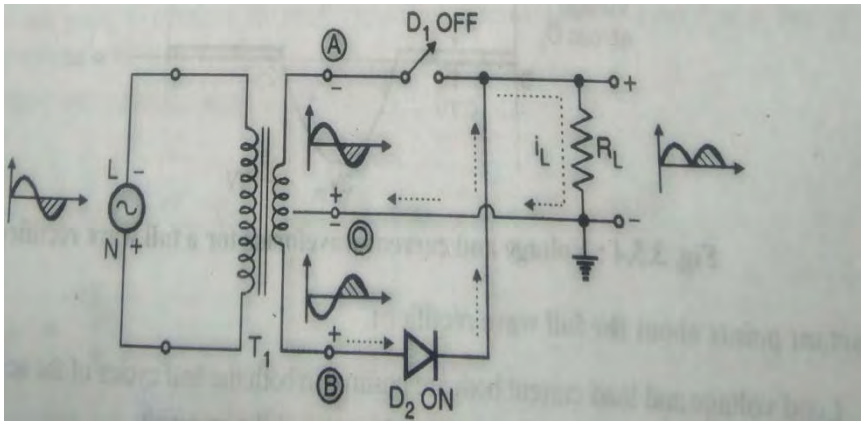
In the **+ve half cycle** of ac supply, the polarities of the secondary induced voltages are as shown in fig. It shows that V_{AO} is positive & V_{BO} is negative.

- Due to the centre tapped secondary, V_{AO} and V_{BO} are always equal & opposite to each other.
- Hence diode D_1 is forward bias & D_2 is reversed biased . The load current starts flowing from A, through D_1, load resistance R_L back to point O as shown in figure.

- The instantaneous load voltage is +ve and approximately equal to V_{AO} . As the load is purely resistive , the load current i_L has the same shape as the load voltage.



In the -ve half cycle of ac supply, the polarities of the secondary induced voltages are as shown in fig. It shows that V_{BO} is positive & V_{AO} is negative.

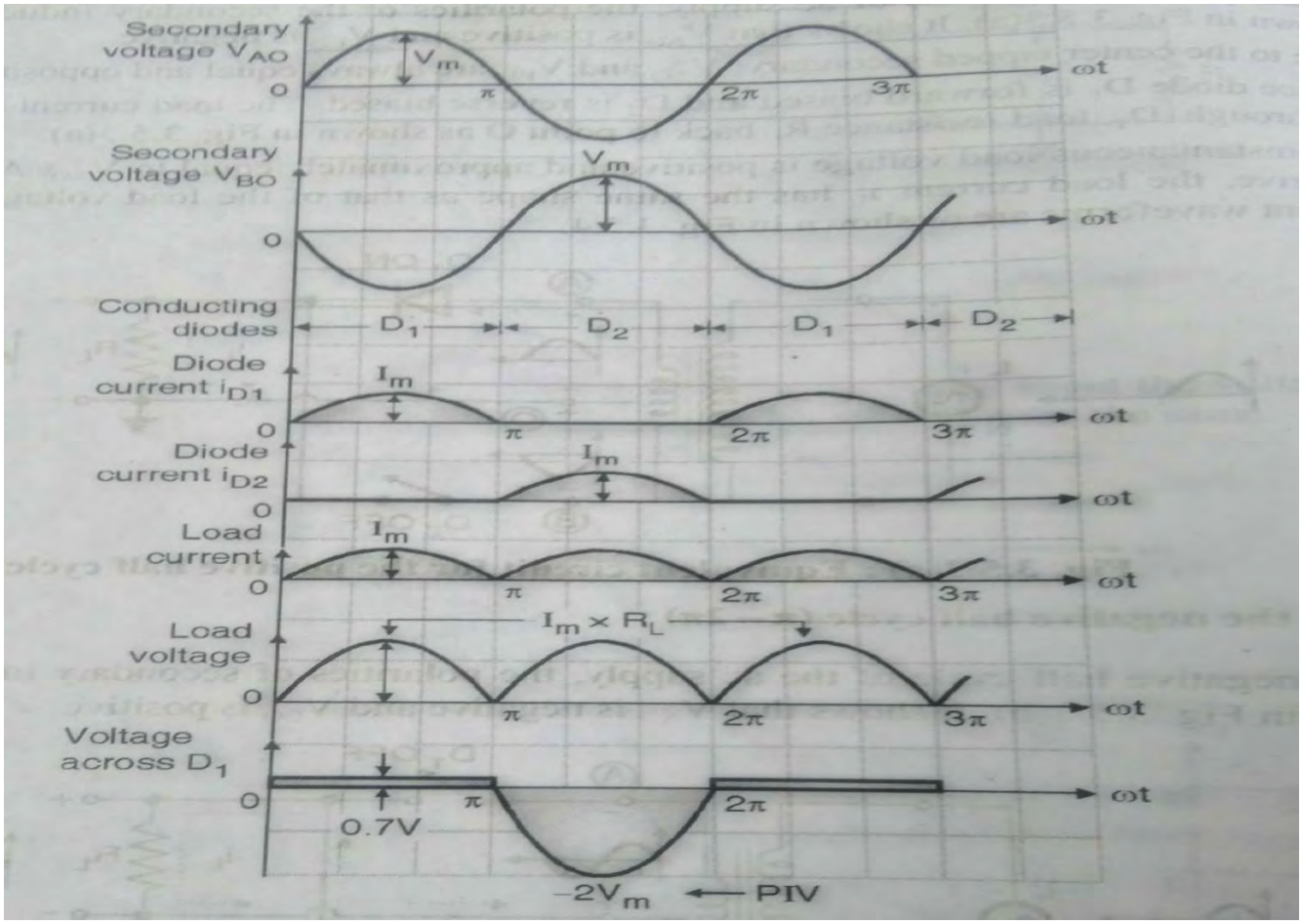


- Due to the centre tapped secondary, V_{AO} and V_{BO} are always equal & opposite to each other.
- Hence diode D_2 is forward bias & D_1 is reversed biased . The load current starts flowing from B, through D_2, load resistance R_L back to point O as shown in figure.
- The direction of load current i_L is same as that in the positive half cycle. It means even in negative half cycle the load current continues to be positive.

Waveforms

As shown in the fig. we have

1. Load voltage & load current both are positive in both the half cycles of the ac supply.
2. Output voltage is available in both the half cycles of the ac supply.
3. The full wave rectifier circuit consists of two half wave rectifier, which work independently feed the common load.

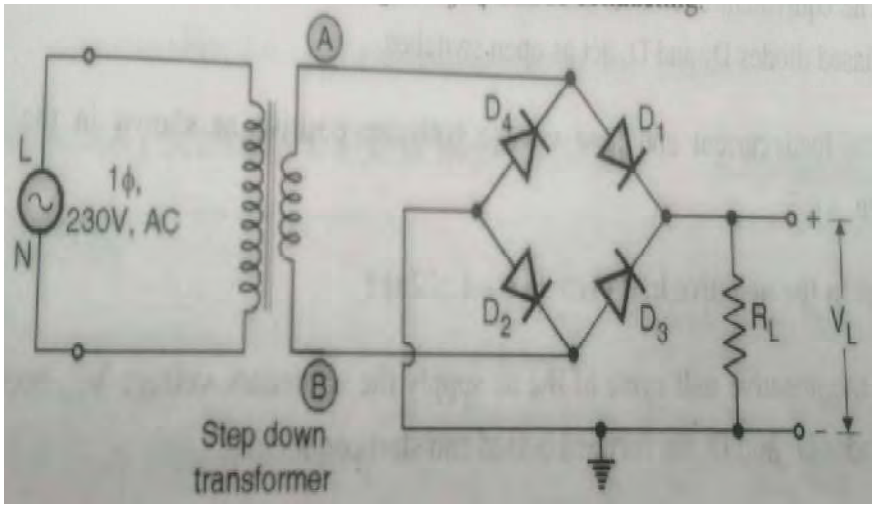


Bridge Rectifier

The disadvantages of the full wave rectifier such as high PIV and compulsory use of centre tapped transformer are overcome in bridge rectifier.

The circuit configuration is shown in fig. , having four diode connected to form a bridge.

The Centre tapped input transformer is not required. The input transformer T_1 shown in fig. is step down transformer.

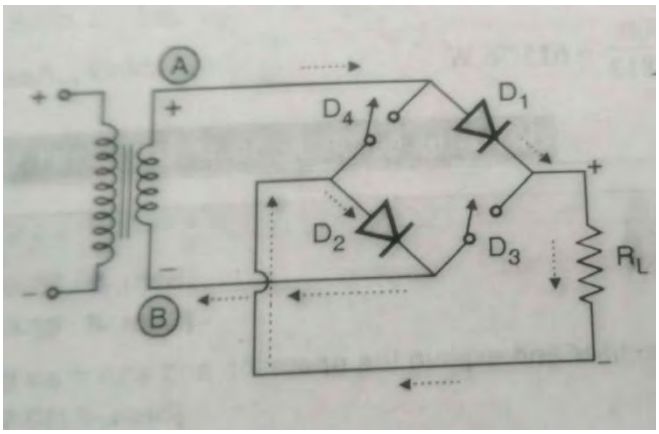


Bridge rectifier offers full wave rectification . The diodes conduct in pairs i.e. at any given instant of time , one pair of diode either D_1, D_2 or D_3 , D_4 will be conducting.

Operation of the Bridge Rectifier

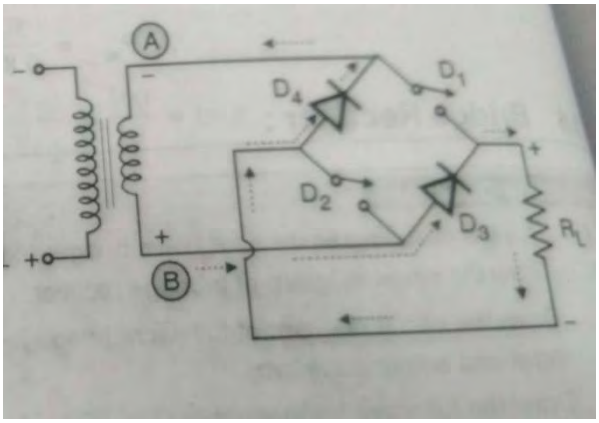
Operation of bridge rectifier can be explained in two half cycles of the AC Supply Voltage as follow :

Operation in Positive Half Cycle



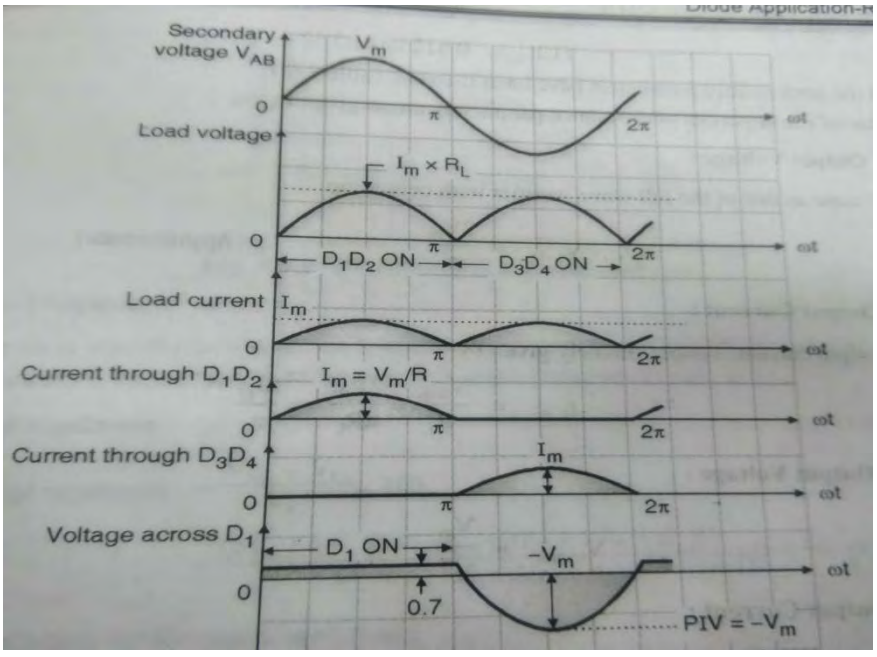
- In the +ve half cycle of the ac supply the secondary voltage V_{AB} is positive. Therefore diodes D_1 & D_2 are forward biased whereas D_3 & D_4 are reversed biased
- The equivalent circuit is shown in fig. The reverse biased diodes D_3 & D_4 act as open switches.
- The Load voltage & current both are positive.

Operation in Negative Half Cycle



- In the -ve half cycle of the ac supply the secondary voltage V_{AB} is negative. Therefore diodes D_3 & D_4 are forward biased whereas D_1 & D_2 are reversed biased
- The equivalent circuit is shown in fig. The reverse biased diodes D_1 & D_2 act as open switches.
- The Load voltage & current both are positive.

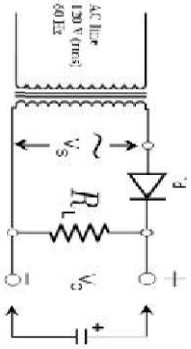
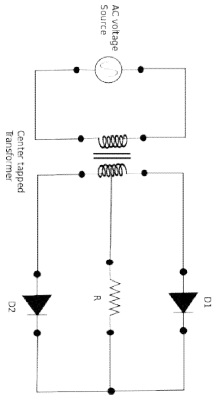
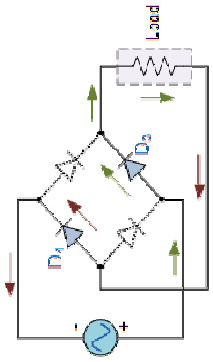
Waveforms



Q.11. How full wave rectifier is better than half wave rectifier ? [Important]

Or

Differentiate between half-wave and full-wave rectification. [Kanpur 2012]

S.No.	Parameters	HWR	FWR	Bridge Rectifier
1.	DC or average load current(I_{dc})	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
2.	Max^m average load voltage (V_{dc})	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
3.	RMS load current I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
3.	RMS load voltage V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
4	DC load power	$\frac{I_m^2}{\pi^2}R_L$	$\frac{4I_m^2}{\pi^2}R_L$	$\frac{4I_m^2}{\pi^2}R_L$
6	Maximum rectification efficiency (η)	40%	81.2 %	81.2%
7	Ripple frequency	121 %	48%	48%
8	No. of diodes used	One	Two	Four
9	Centre tap transformer	Not Required	Very much required	Not Required
10	PIV	V_m	2 V_m	V_m
11	Circuit diagram			

Q.12. Describe the working of a full wave rectifier and discuss the use of filters to avoid ripples. Give the diagram to illustrate your answer.
[Important]

Related Short Answer Questions

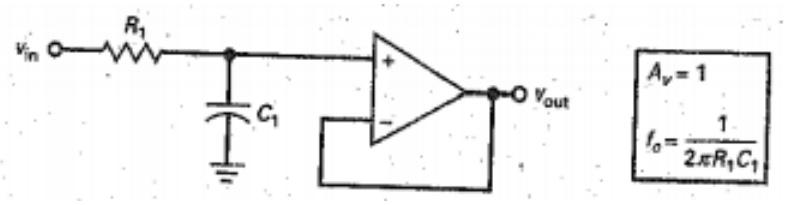
(i) What is filter circuit [Important]
(ii) What is the necessity of having filter in a power supply ? [Important]

For full wave ref to Q.7.

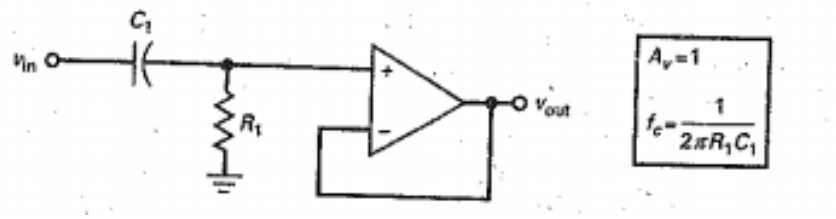
Filter

A filter is a circuit that passes one band of frequencies while rejecting another. Filters can separate desired signals from undesired signals, block interfering signals, enhance speech and video, and alter signals in other ways. A filter can either passive or active. Passive filters are built with resistors, capacitors and inductors. They are generally used above 1MHz. have no power gain, and are relatively difficult to tune. Active filters are built with resistors , capacitors and op amps. They are useful below 1 MHz, have power gain, and are relatively easy to tune.
There are five types of filter

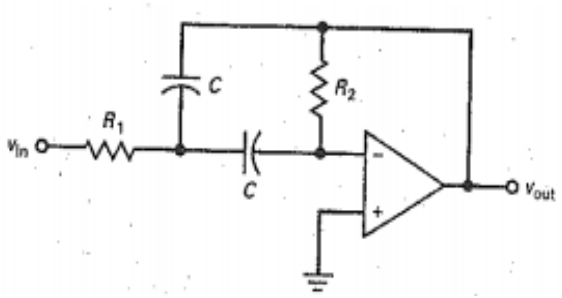
(i) Low Pass Filter



(ii) High Pass Filter



(iii) Band Pass Filter

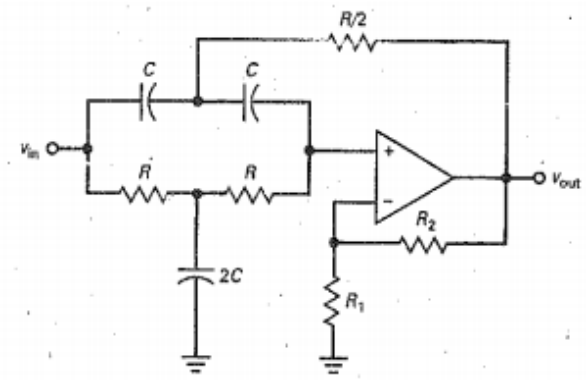


$$A_v = \frac{-R_2}{2R_1}$$

$$Q = 0.5\sqrt{\frac{R_2}{R_1}}$$

$$f_0 = \frac{1}{2\pi C\sqrt{R_1 R_2}}$$

(iv) Band Reject Filter

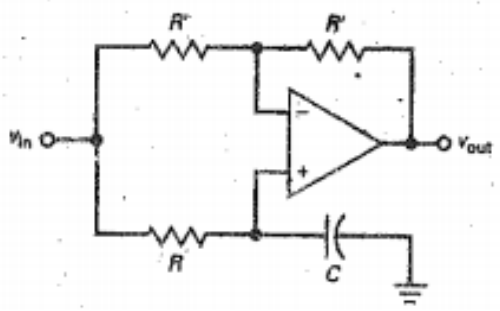


$$A_v = \frac{R_2}{R_1} + 1$$

$$Q = \frac{0.5}{2 - A_v}$$

$$f_0 = \frac{1}{2\pi RC}$$

(v) All Pass Filter



$$A_v = 1$$

$$f_0 = \frac{1}{2\pi RC}$$

$$\phi = -2 \arctan \frac{f}{f_0}$$

Numerical

Q.1. A full wave rectifier uses two crystal diodes each having 10Ω internal resistance . The maximum a.c. voltage across each diode is 70.7 volts. Find the d.c. output voltage across the load resistance through which rms value of load current is 50mA.

Exp: The full wave rectifier uses two diode i.e. type is centre taped

Diode Resistance(R_d) = 10Ω

If V_m is the peak voltage of input , then maximum voltage across diode is $2V_m$

i.e. $2V_m$= 70.7

∴ V_m= 70.7/2 = 35.35 volts

∵ rms current across the load with diode resistance (R_D) & load resistance(R_L) is

$$I_{rms} = I_m/\sqrt{2} = \frac{V_m}{\sqrt{2}\,(R_F+R_L)} = 50\text{mA} \qquad (1)$$

$$\Rightarrow \quad \frac{35.35}{\sqrt{2}\,(R_F+R_L)} = 50\text{mA} \qquad \{\text{From eq. (1)}\}$$

$$\therefore R_d + R_L = 500\ \Omega$$

$$\Rightarrow 10\Omega + R_L = 500\ \Omega$$

$$\therefore\ R_L = 490\ \Omega$$

$$\Rightarrow \quad I_m/\sqrt{2} = 50\text{mA} \qquad \{\text{From eq. (1)}\}$$

$$\therefore I_m = 50\sqrt{2}\ \text{mA}$$

DC output voltage across load $V_{dc} = \frac{2I_mR_L}{\pi}$

$$\Rightarrow \quad V_{dc} = \frac{2\ x\ 50\sqrt{2}\ \text{x}\ 490\ \Omega}{\pi} = \frac{1.414\ x\ 49}{\pi}\ volt$$

$$\therefore V_{dc} = 22.06\ volt \ \text{Ans}$$

Q.2. Calculate the current through 48 Ω resistor in the circuit shown in figure below. Each diode is made of silicon and the forward resistance of each diode is equal to 1Ω .

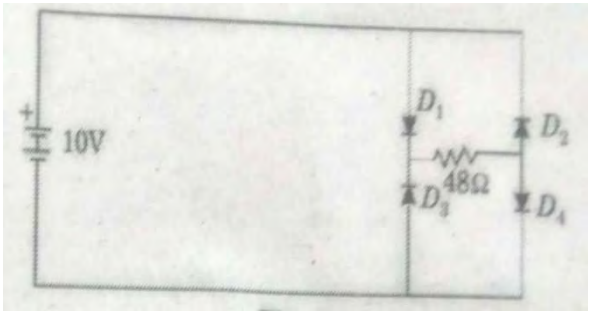
Exp: In the given circuit D_1 & D_4 are forward bias

for the given bias .

$$\therefore R_{resultant} = 1 + 48 + 1 = 50\Omega$$

∴ Current through 48 Ω = 10V / 50 Ω

$$= 1/5 = 0.2\text{Amp} \ \text{Ans}$$



Q.3. A full wave rectifier uses two diodes. The internal resistance of each diode may be assumed constant at 20 Ω. The transformer R.M.S. secondary voltage from centre tap to each end of secondary is 50 volt and load resistance is 980 Ω.

Calculate:

(i) The mean load current (or d.c. load current)

(ii) The R.M.S. value of load current. **[Kanpur 2012]**

Exp: The full wave rectifier uses two diode i.e. type is centre taped

Diode Resistance(R_d) = 20Ω

Load resistance (R_L) = 980 Ω

Max^m load current (I_m) = $\frac{V_m}{(R_F+R_L)} = \frac{70.7V}{(20\Omega+980\ \Omega)} =$ 70.7mA

RMS load current (I_{rms}) = $\frac{I_m}{\sqrt{2}} = \frac{70.7\text{mA}}{\sqrt{2}} =$ 50mA

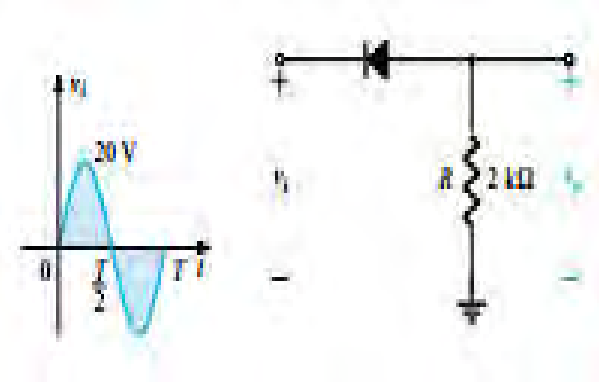
Mean load current (I_{dc}) = $\frac{2I_m}{\pi} = \frac{70.7\text{mA}}{\pi} =$ 45mA

Q.4. (a) Sketch the output v_o and determine the dc level of the output for the network of Fig.

(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.

Exp: The diode will conduct during the -ve part of

the input as shown in fig.



(a) For the full period , the dc level is

V_{dc} = -0.318V_m

= -0.318 x 20V

= -6.36V Ans

The negative sign indicates that the polarity of the output is opposite to the defined polarity

(b) If the general diode replaces ideal diode

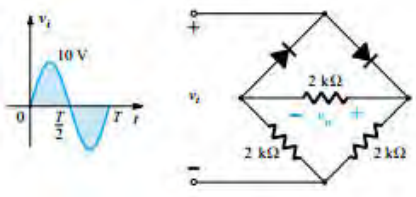
∴ V_{dc} ≈ -0.318 (V_m – 0.7V)

≈ -0.318 (20 – 0.7V)

≈ -0.318 x 19.3

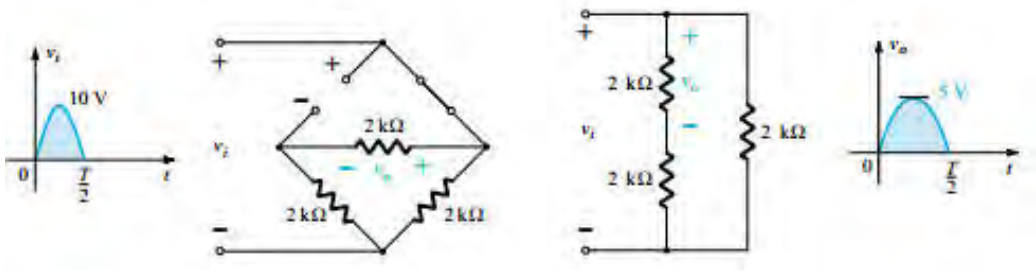
≈ -6.14V Ans

Q. 5. Determine the output waveform for the network of fig. and calculate the output dc level and the required PIV of each diode.



Exp: The network shown in the question , for the positive region of the input voltage will appear as in

fig(a)



(a) (b) (c)

Redrawing the network as in fig. (b) , We have

$v_O = 0.5\ v_i$

$v_{O(max)} = 0.5 \times 10 = 5$ Volt

v_O will appear as shown in fig.(c) .

Since the circuit is not a centre taped , and acting as a full wave rectifier

∴ Output DC level $= 0.636\ (5V) = 3.18$ V

∴ PIV of each diode $= 5$Volt Ans

Q.6. Determine I, V_1, V_2 and V_0 for the series dc configuration shown in figure

Exp: Applying KVL for the given circuit , we have

$-10 + IR_1 + 0.7 + IR_2 - 5 = 0$

$I(R_1 + R_2) = 15 - 0.7$

$I(4.7k\Omega + 2.2k\Omega) = 14.3$

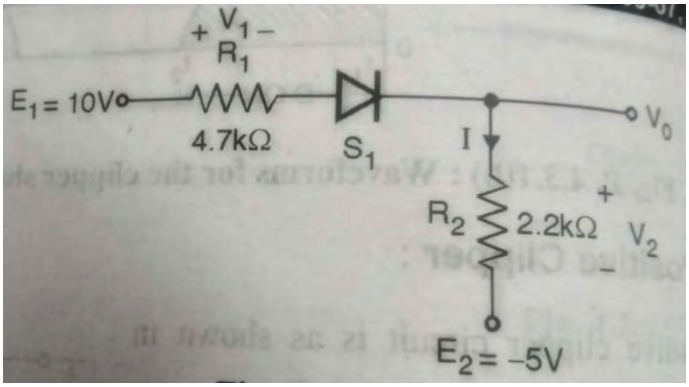
$I = 14.3 / 6.9\ k\Omega$

$= 2.0724$ mA Ans

$V_1 = 4.7k\Omega \times 2.0724$ mA

$= 9.740$ V Ans

$V_2 = 2.2k\Omega \times 2.0724$ mA $= 4.56$ V Ans



$\because V_0 = V_2 - 5\ V$

$\therefore V_0 = 4.56\ V - 5V = -0.4V$ Ans

Chapter-9
Miscellaneous

The four layer Diode

A thyristor is a semiconductor device that uses internal positive feedback to produce latching action. The four-layer diode, also called a Schockley diode, is the simplest thyristor. Breakdown closes it, and low-current drop-out opens it.

Thyristor Family

The P-N-P-N devices with zero , one or two gates constitute the basic thyristor .The complete list of thyristor family includes diac(bidirectional diode thyristor), triac(bidirectional triode thyristor), SCR(silicon controlled rectifier), schockely diode, SCS(silicon controlled switch), SBS (silicon biletral switch), SUS (silicon unilateral switch) also known as complementary SCR or CSCR , LASCR(light activated SCR), LAS (light activated switch) and LASCS(light activated SCS).

The Silicon Controlled Rectifier

The silicon controlled rectifier(SCR) is three terminal four-layer semiconductor device and is most widely used thyristor . It can switch very large currents on and off . To turn it on , we need to apply a minimum gate trigger voltage and current. To turn it off, we need to reduce the anode voltage to almost zero.

Turn on methods in SCR

SCR can be switched on either by increasing the forward voltage beyond forward break over voltage V_{FBO} or by applying a positive gate signal when the device is forward biased. Of these two methods , the latter , called the gate –control method, is used as it is more efficient & easy to implement for power control.

Turn off methods in SCR

Once the SCR is fired, it remains ON even when triggering pulse is removed . The ability of the SCR to remain ON even when gate current is removed is referred to as latching . So SCR cannot be turned off by simply removing the gate pulse. There three methods of switching –off the SCR , namely natural commutation , reverse bias turn-off , and gate turn-off.

SCR as a Rectifier

SCRs are very useful in ac circuits where they serve as rectifier whose output current can be controlled by controlling the gate current. The ac supply voltage to be rectified is applied to the primary of the transformer ensuring that the negative voltage appearing at the secondary of the transformer is less than reverse breakdown voltage of the SCR.

Bidirectional Thyristors

The diac can latch current in either direction . It is open until the voltage across it exceeds the breakdown

Unijunction Transistor

The **Unijunction Transistor** or **UJT** for short, is a solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triacs for AC power control type applications.

Integrated Circuit

A device that contains its own transistors , resistor and diode. A complete IC using these microscopic components can be produced in the space occupied by a discrete transistor.

Classification of ICs

On the fabrication techniques used , ICs can be divided into three classes

Monolitic ICs : The word ‘monolitic’ is derived from the greek monos , meaning ‘single’ and lithos, meaning ‘stone’. Thus monolithic circuit is built into a single stone or single crystal i.e. in monolithic ICs, all circuit components , (both active & passive) and their interconnections are formed into or on the top of a single chip of silicon.

Thin Film ICs

These devices are larger than monolithic ICs but smaller than discrete circuits. These ICs can be used when power requirement is comparatively higher. These ICs are fabricated by depositing films of conducting material on the surface of a glass or ceramic base.

Thick film ICs

These ICs are manufactured by silk-screen printing techniques are used to create the desire circuit pattern on a ceramic substrate.

Chip Size

On the basis of chip size the ICs are classified as

SSI i.e. small scale integration having 3-10 gates/chip; MSI i.e. medium scale integration having 30-300 gates/chip; LSI i.e. large scale integration having 300-3,000 gates/chip; VLSI i.e. very large scale integration having more than 3,000 gates/chip.

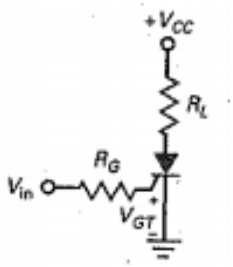
IC packages

For the protection of ICs from external environment and to provide mechanical protection and terminals for electrical connections, various types of packages are used.

Derivation

SCR turn-on :

$V_{in} = V_{GT} + I_{GT}R_G$



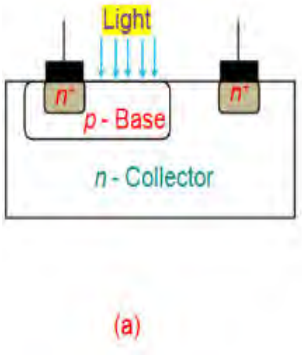
Long & Short Questions

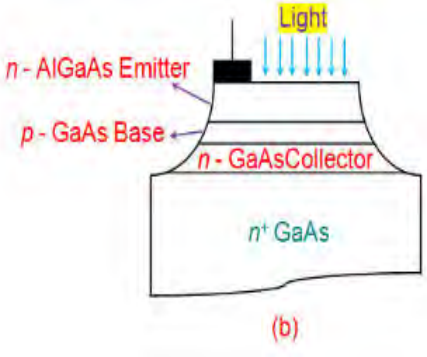
Q.1. Explain the construction and working of phototransistor. [Kanpur 2014]

Or

What are the characteristics of photodiode ? Explain its configuration & uses.

Phototransistors are either tri-terminal (emitter, base and collector) or bi-terminal (emitter and collector) semiconductor devices which have a light-sensitive base region. Although all transistors exhibit light-sensitive nature, these are specially designed and optimized for photo applications.



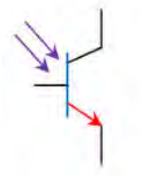


These are made of diffusion or ion-implantation and have much larger collector and base regions in comparison with the ordinary transistors. These devices can be either homojunction structured or heterojunction structured, as shown by Figure a and b, respectively. In the case of homojunction phototransistors, the entire device will be made of a single material-type; either silicon or germanium.

However to increase their efficiency, the phototransistors can be made of non-identical materials (Group III-V materials like GaAs) on either side of the pn junction leading to heterojunction devices. Nevertheless, homojunction devices are more often used in comparison with the hetero junction devices as they are economical.

Circuit symbol

The circuit symbol for npn phototransistors is shown in fig (c) & (d) which is nothing but a transistor (with or without base lead) with two arrows pointing towards the base indicating its sensitivity to light. Similar symbolic representation holds well even in the case of pnp phototransistors with the only change being the arrow at emitter pointing in, instead of out.

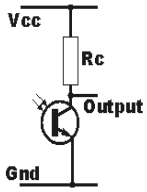


c

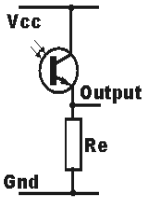
d

The behavior of phototransistors is identical to that of normal transistors except the fact that here the effect brought-about by the base voltage will be experienced due to the incident light. This can be made clearer by analyzing the following points

1. The characteristics of **phototransistors** are similar to those of normal transistors except that they have base current replaced by light intensity. This means that even these devices have three operating regions viz., cut-off, active and saturation. This further implies that the phototransistors can be used for either switching (cut-off and saturation mode dependent) applications or for amplification (active mode operation), just like ordinary transistors.
2. The phototransistors can be configured in two different configurations viz., common collector and common emitter, depending on the terminal which is common between the input and output terminals, similar to normal transistors.



Common emitter phototransistor circuit



Common collector phototransistor circuit

3. A small reverse saturation current, called **dark current**, flows through the phototransistor even in the absence of light whose value increases with an increase in the value of temperature, a property identical to that exhibited by the ordinary transistors.
4. Phototransistors are prone to permanent damage due to breakdown if the voltage applied across the collector-emitter junction increases beyond its breakdown voltage, just as in the case of normal transistors.

Generally, in the case of phototransistor circuits, the collector terminal will be connected to the supply voltage and the output is obtained at the emitter terminal while the base terminal, if present, will be left unconnected. Under this condition, if light is made to fall on the base region of the phototransistor, then

it results in the generation of electron-hole pairs which give rise to base current, nothing but the photo-current, under the influence of applied electric field. This further results in the flow of emitter current through the device, resulting in the process of amplification. This is because, here, the magnitude of the photo-current developed will be proportional to the luminance and will be amplified by the gain of the transistor leading to a larger collector current.

The output of the **phototransistor** depends on varies factors like

- Wavelength of the incident light
- Area of the light-exposed collector-base junction
- DC current gain of the transistor.

Further, the characteristics of a particular phototransistor can be expressed in terms of its

- Luminous sensitivity defined as the ratio of photoelectric current to the incident luminous flux
- Spectral response which decides the longest wavelength which can be used as the sensitivity of the phototransistors is a function of wavelength
- Photoelectric gain which indicates its efficiency of converting light into an amplified electrical signal
- Time constant which influences its response time.

However, it is important to note that the speed of response and the phototransistor gain are inversely proportional to each other, meaning which one decreases if the other increases.

Phototransistor characteristics

Photo transistor has a high level of gain resulting from the transistor action. For homo-structures, i.e. ones using the same material throughout the device, this may be of the order of about 50 up to a few hundred. However for the hetero-structure devices, the levels of gain may rise to ten thousand. Despite their high level of gain the hetero-structure devices are not widely used because they are considerably more costly to manufacture. A further advantage of all phototransistors when compared to the avalanche photodiode, another device that offers gain, is that the phototransistor has a much lower level of noise.

One of the main disadvantages of the phototransistor is the fact that it does not have a particularly good high frequency response. This arises from the large capacitance associated with the base-collector junction. This junction is designed to be relatively large to enable it to pick up sufficient quantities of light. For a typical homo-structure device the bandwidth may be limited to about 250 kHz. Hetero-junction devices have a much higher limit and some can be operated at frequencies as high as 1 GHz.

The characteristics of the photo-transistor under different light intensities. They are very similar to the characteristics of a conventional bipolar transistor, but with the different levels of base current replaced by the different levels of light intensity.

There is a small amount of current that flows in the photo transistor even when no light is present. This is called the dark current, and represents the small number of carriers that are injected into the emitter. Like the photo-generated carriers this is also subject to the amplification by the transistor action. The phototransistor can be used in a variety of circuits and in a number of ways dependent upon the application. Being a low cost device the phototransistor is widely used in electronic circuits and it is also easy to incorporate.

Advantages of Phototransistor

1. Simple, compact and less expensive.
2. Higher current, higher gain and faster response times in comparison with photodiodes.
3. Results in output voltage unlike photo resistors.
4. Sensitive to a wide range of wavelengths ranging from ultraviolet (UV) to infrared (IR) through visible radiation.
5. Sensitive to large number of sources including incandescent bulbs, fluorescent bulbs, neon bulbs, lasers, flames and sunlight.
6. Highly reliable and temporally stable.
7. Less noisy when compared to avalanche photodiodes.
8. Available in wide variety of package types including epoxy-coated, transfer-molded and surface mounted.

Disadvantages of Phototransistor

- Cannot handle high voltages if made of silicon.
- Prone to electric spikes and surges.
- Affected by electromagnetic energy.
- Do not permit the easy flow of electrons unlike electron tubes.
- Poor high frequency response due to a large base-collector capacitance.
- Cannot detect low levels of light better than photodiodes.

Applications of Phototransistor

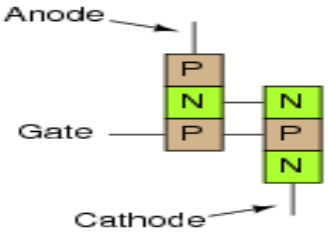
- Object detection
- Encoder sensing
- Automatic electric control systems such as in light detectors
- Security systems
- Punch-card readers
- Relays
- Computer logic circuitry
- Counting systems
- Smoke detectors
- Laser-ranging finding devices
- Optical remote controls
- CD players
- Astronomy
- Night vision systems
- Infrared receivers
- Printers and copiers
- Cameras as shutter controllers
- Level comparators

Q.2. Draw the construction and explain the characteristics curve of an SCR showing how forward voltage depends on the value of gate current.
Also define the terms related to SCR

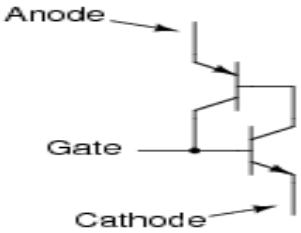
Related short Questions

(i) Write short note on silicon controlled Rectifier (SCR). [Kanpur 2014]

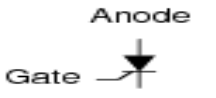
The silicon controlled rectifier(SCR) is three terminal four-layer semiconductor device and is most widely used thyristor . It can switch very large currents on and off . To turn it on , we need to apply a minimum gate trigger voltage and current. To turn it off, we need to reduce the anode voltage to almost zero.



Physical diagram



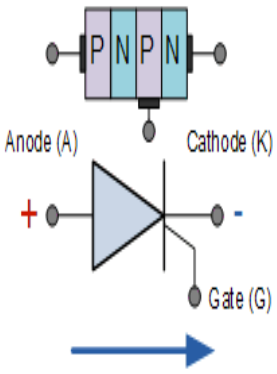
Equivalent schematic



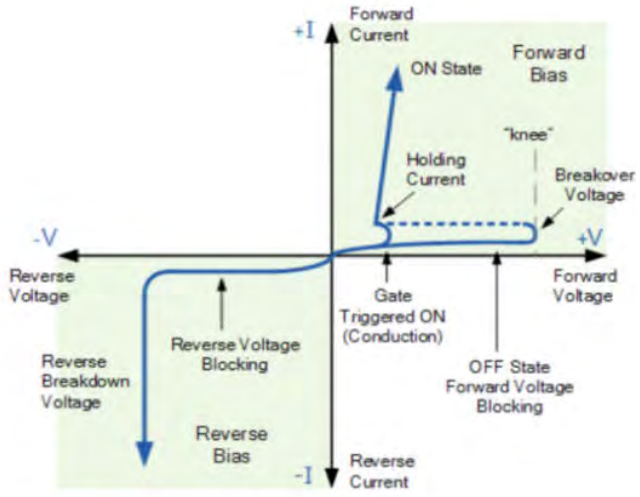
Schematic symbol

V-I Characteristics of SCR

It is the curve between anode-cathode voltage (V) and anode current (I) of an SCR at constant gate current.



(a)



(b)

Forward Characteristics

When anode is positive w.r.t. cathode, the curve between V and I is called the forward characteristics.

In fig.(b) is the forward characteristics of SCR at I_G=0.If the supply voltage is increased from zero, a point reached when the SCR starts conducting.
Under this condition, the voltage across SCR suddenly drops as shown by dotted curve and most of supply voltage appears across the load resistance R_L .If proper gate current is made to flow, SCR can conduct at much smaller supply voltage.

Reverse Characteristics

When anode is negative w.r.t. cathode, the curve between V and I is known as reverse characteristics. The reverse voltage does come across SCR when it is operated with a.c. supply. If the reverse voltage is gradually increased, at first the anode current remains small (i.e. leakage current) and at some reverse voltage, avalanche breakdown occurs and the SCR starts conducting heavily in the reverse direction as shown by the curve .

This maximum reverse voltage at which SCR starts conducting heavily is known as **reverse breakdown voltage.**

SCR in Normal Operation

To operate SCR under normal conditions

- The supply voltage is generally much less than breakover voltage.
- The SCR is turned on by passing appropriate amount of gate current (a few mA) and not by break over voltage.
- When SCR is operated from a.c. supply, the peak reverse voltage which comes during negative half-cycle should not exceed the reverse breakdown voltage.
- When SCR is to be turned OFF from the ON state, anode current should be reduced to holding current.
- If gate current is increased above the required value, the SCR will close at much reduced supply voltage.

Important terms in the V-I Characteristics of SCR

1. Breakover voltage
2. Peak reverse voltage
3. Holding current
4. Forward current rating
5. Circuit fusing rating

Breakover Voltage

It is the minimum forward voltage, gate being open, at which SCR starts conducting heavily i.e. turned on.
If the breakover voltage of an SCR is 200 V, it means that SCR can block a forward voltage (i.e. SCR remains open) as long as the supply voltage is less than 200 V. If the supply voltage is more than this value, then SCR will be turned on.
In practice, the SCR is operated with supply voltage less than breakover voltage and it is then turned on by means of a small voltage applied to the gate.
Commercially available SCRs have breakover voltages from about 50 V to 500 V.

Peak Reverse Voltage (PRV)

It is the maximum reverse voltage (cathode positive w.r.t. anode) that can be applied to an SCR without conducting in the reverse direction.

PRV is an important consideration while connecting an SCR in an a.c. circuit. During the negative half of a.c. supply, reverse voltage is applied across SCR. If PRV is exceeded, there may be avalanche breakdown and the SCR will be damaged if the external circuit does not limit the current. Commercially available SCRS have PRV ratings upto 2.5 kV.

Holding Current

It is the maximum anode current, gate being open, at which SCR is turned OFF from ON condition. When SCR is in the conducting state, it cannot be turned OFF even if gate voltage is removed. The only way to turn off or open the SCR is to reduce the supply voltage to almost zero at which point the internal transistor comes out of saturation and opens the SCR.

The anode current under this condition is very small (a few mA) and is called holding current.

Thus, if an SCR has a holding current of 5mA, it means that if anode current is made less than 5 mA, then SCR will be turned off.

Forward Current Rating

It is the maximum anode current that an SCR is capable of passing without destruction. Every SCR has a safe value of forward current which it can conduct. If the value of current exceeds this value, the SCR may be destroyed due to intensive heating at the junction.

For example, if an SCR has a forward current rating of 40 A, it means that the SCR can safely carry only 40 A. Any attempt to exceed this value will result in the destruction of the SCR.

Commercially available SCRs have forward current ratings from about 30A to 100A.

Circuit Fusing (I^2t) Rating

It is the product of square forward surge current and the time of duration of the surge i.e.

$$\text{Circuit fusing rating} = I^2t$$

The circuit fusing rating indicates the maximum forward surge current capability of SCR.

For example, consider an SCR having circuit fusing rating of 90 A^2s. If this rating is exceeded in the SCR circuit , the device will be destroyed by excessive power dissipation.

Q.3. Explain construction and working of silicon controlled rectifier. Draw the V-I characteristic curve . [Kanpur 2016]

Or

Discuss SCR as a half wave rectifier.

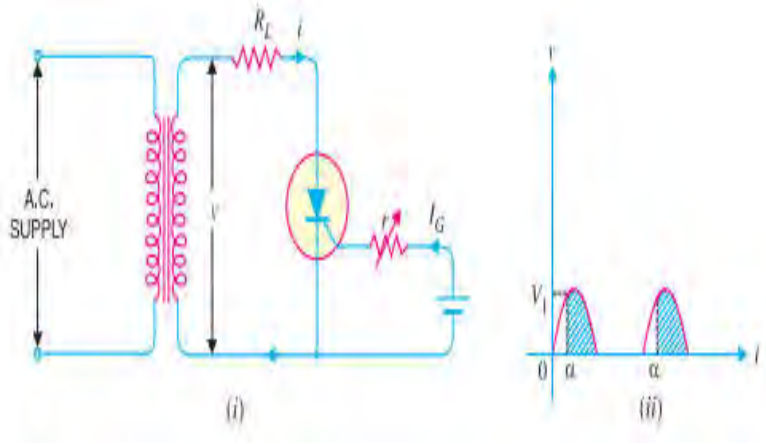
Or

Discuss SCR as a full wave rectifier.

For construction refer to Q.2

SCR as a half wave rectifier

One important application of an SCR is the controlled half-wave rectification. Fig. (i) shows the circuit of an SCR half-wave rectifier. The a.c. supply to be rectified is supplied through the transformer. The load resistance R_L is connected in series with the anode. A variable resistance r is inserted in the gate circuit to control the gate current.



Operation.

The a.c. supply to be converted into d.c. supply is applied to the primary of the transformer. Suppose the peak reverse voltage appearing across secondary is less than the reverse breakdown voltage of the SCR. This condition ensures that SCR will not break down during negative half-cycles of a.c. supply. The circuit action is as follows :

1. During the negative half-cycles of a.c. voltage appearing across secondary, the SCR does not conduct regardless of the gate voltage. It is because in this condition, anode is negative w.r.t. cathode and also PRV is less than the reverse breakdown voltage.
2. The SCR will conduct during the positive half-cycles provided proper gate current is made to flow. The greater the gate current, the lesser the supply voltage at which SCR is turned ON. The gate current can be changed by the variable resistance r as shown in Fig. (i).
3. Suppose that gate current is adjusted to such a value that SCR closes at a positive voltage V_1which is less than the peak voltage Vm. Referring to Fig. (ii), it is clear that SCR will start conducting when secondary a.c. voltage becomes V_1in the positive half-cycle.
4. Beyond this, the SCR will continue to conduct till voltage becomes zero at which point it is turned OFF.
5. Again at the start of the next positive half-cycle, SCR will start conducting when secondary voltage becomes V_1
6. Referring to Fig. (ii), it is clear that firing angle is α i.e. at this angle in the positive half-cycle, SCR starts conduction. The conduction angle is φ(= 180° − α).

Average Voltage

Ref. to fig. (i) , let $v = V_m sin\Theta$ be the alternating voltage that appears across the secondary. Let α be the firing angle. It means that rectifier will conduct from α to 180^0 (π)during the positive half cycles.

∴ Average output , $V_{average} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \, sin\Theta \, d\Theta = -\frac{V_m}{2\pi}[cos\Theta]_{\alpha}^{\pi}$

$$V_{average} = -\frac{V_m}{2\pi}[cos\pi - cos\alpha] = -\frac{V_m}{2\pi}[-1 - cos\alpha] = \frac{V_m}{\pi}[1 + cos\alpha]$$

Average current , $I_{av} = V_{av}/R_L = \frac{V_m}{2\pi R_L}[1 + cos\alpha]$

- If the firing angle $\alpha = 0^0$, then full positive half-cycle will apper across the load R_L and the output current becomes :

$$I_{av} = \frac{V_m}{2\pi R_L}[1 + cos0^0] = \frac{V_m}{\pi R_L}$$

This is the value of average current for ordinary half-wave rectifier. This is expected since the full positive half-cycle is being conducted**.**

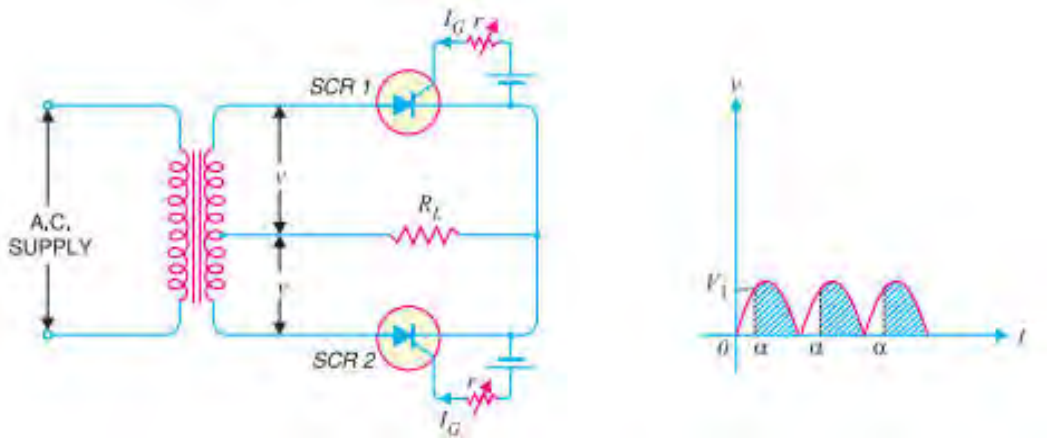
- If the firing angle $\alpha = 90^0$, then the average current is given by :

$$I_{av} = \frac{V_m}{2\pi R_L}[1 + cos90^0] = \frac{V_m}{2\pi R_L}$$

This shows that greater the firing angle α , the smaller is the average current and vice-versa.

SCR Full-Wave Rectifier

Fig. (i) shows the circuit of SCR full-wave rectifier. It is exactly like an ordinary centre-tap circuit except that the two diodes have been replaced by two SCRs. The gates of both SCRs get their supply from two gate controls. One SCR conducts during the positive half-cycle and the other during the negative half-cycle. Consequently, full-wave rectified output is obtained across the load.



(i) **(ii)**

Operation.

- The angle of conduction can be changed by adjusting the gate currents. Suppose the gate currents are so adjusted that SCRs conduct as the secondary voltage (across half winding) becomes V_1.
- During the positive half-cycle of a.c. across secondary, the upper end of secondary is positive and the lower end negative. This will cause SCR1 to conduct. However, the conduction will start only when the voltage across the upper half of secondary becomes V_1 as shown in Fig. (ii). In this way, only shaded portion of positive half-cycle will pass through the load.
- During the negative half-cycle of a.c. input, the upper end of secondary becomes negative and the lower end positive. This will cause SCR2 to conduct when the voltage across the lower half of secondary becomes V_1
- It may be seen that current through the load is in the same direction (d.c.) on both half-cycles of input a.c. The obvious advantage of this circuit over ordinary full-wave rectifier

circuit is that by adjusting the gate currents, we can change the conduction angle and hence the output voltage.

Average Voltage

Ref. to fig. (i) , let $v = V_m sin\Theta$ be the alternating voltage that appears between centre tap 7 either end of secondary. Let α be the firing angle.

Average output $V_{average} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \, sin\Theta \, d\Theta = -\frac{V_m}{\pi}[cos\Theta]_{\alpha}^{\pi}$

$V_{average} = -\frac{V_m}{\pi}[cos\pi - cos\alpha] = -\frac{V_m}{\pi}[-1 - cos\alpha] = \frac{V_m}{\pi}[1 + cos\alpha]$

This value is double that of a half-wave rectifier. It is expected since now negative half-cycle is also rectified.

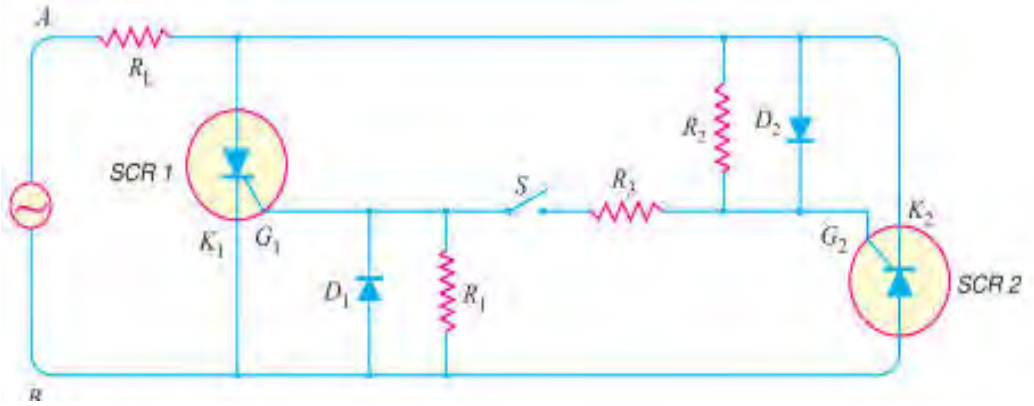
Average current , $I_{av} = V_{av}/R_L = \frac{V_m}{\pi R_L}[1 + cos\alpha]$

Q.4. What are the applications of SCR ?

The ability of an SCR to control large currents in a load by means of small gate current makes this device useful in switching and control applications. Some of the important applications of SCR are

SCR as static contactor

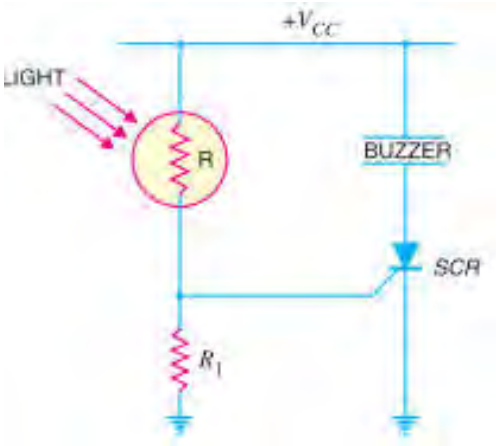
An important application of SCR is for switching operations. As SCR has no moving parts, therefore, when it is used as a switch, it is often called a static contactor



- Fig. shows the use of SCR to switch ON or OFF a.c. power to a load R_L. Resistances R_1 and R_2 are for the protection of diodes D_1 and D_2 respectively. Resistance R_3 is the gate current limiting resistor. To start the circuit, switch is closed.
- During the positive half-cycle of a.c. supply, end A is positive and end B is negative. Then diode D_2 sends gate current through SCR1. Therefore SCR1 is turned ON while SCR2 remains OFF as its anode is negative w.r.t. cathode. The current conduction by SCR1 follows the path AR_LK_1BA.
- Similarly, in the next half-cycle, SCR2 is turned ON and conducts current through the load.
- It may be seen that switch S handles only a few mA of gate current to switch ON several hundred amperes in the load R_L. This is a distinct advantage over a mechanical switch.

Overlight detector.

Fig. shows the use of SCR for overlight detection. The resistor R is a photo-resistor, a device whose resistance decreases with the increase in light intensity.



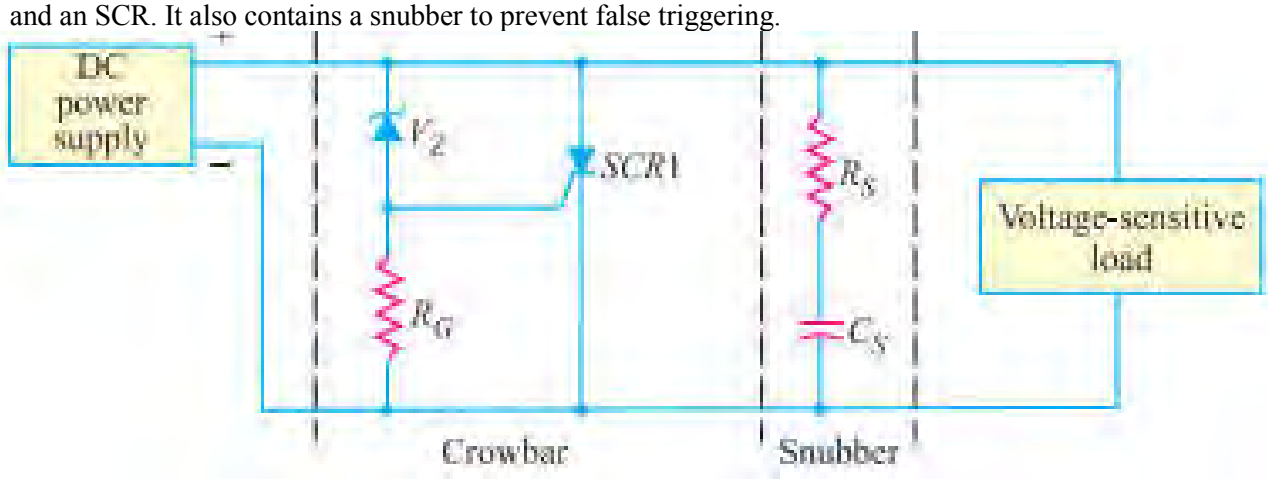
Operation

When the light falling on R has normal intensity, the value of R is high enough and the voltage across R_1 is insufficient to trigger the SCR. However, when R receives high intensity of light, its resistance decreases

The voltage drop across R_1 becomes high enough to trigger the SCR. Consequently, the buzzer sounds the alarm. It may be noted that even if the strong light disappears, the buzzer continues to sound the alarm. It is because once the SCR is fired, the gate loses all control.

SCR Crowbar.

A crowbar is a circuit that is used to protect a voltage-sensitive load from excessive d.c. power supply output voltages. fig. shows the SCR crowbar circuit. It consists of a zener diode, a gate resistor R_G and an SCR. It also contains a snubber to prevent false triggering.



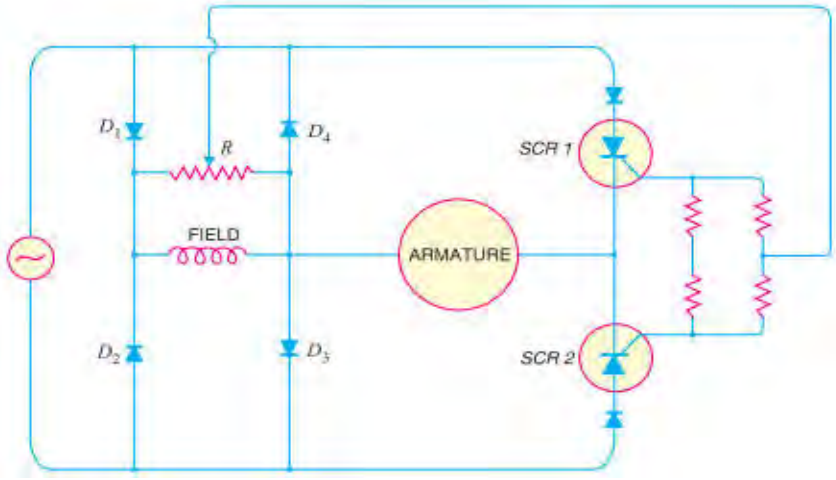
Operation.

- Under normal conditions, the zener diode and the SCR are OFF. With zener diode being in cutoff, there is no current through R_G and no voltage drop occurs across this resistor. This means that the gate of SCR is at 0V so that the SCR is in the off state.
- Therefore, as long as zener diode is off, the SCR behaves as an open and will not affect either the d.c. power supply or the load.
- Suppose the output voltage from the d.c. power supply suddenly increases. This causes the zener diode to break down and conduct current.
- As the current flows through the zener diode, voltage is developed across resistor R_G which causes the SCR to conduct current. When the SCR conducts, the voltage source is shorted by the SCR. The supply voltage fuse blows out and the load is protected from overvoltage.

SCRs for speed control of d.c. shunt motor.

- The conventional method of speed control of d.c. shunt motor is to change the field excitation. But change in field excitation changes the motor torque also. This drawback is overcome in SCR control as shown in Fig. 20.21. Diodes D_1 , D_2, D_3 and D_4 form the bridge.

- This bridge circuit converts a.c. into d.c. and supplies it to the field winding of the motor. During the positive half-cycle of a.c. supply, SCR1 conducts because it gets gate current from bridge circuit as well as its anode is positive w.r.t. cathode. The armature winding of the motor gets current. The angle of conduction can be changed by varying the gate.



current. During the negative half-cycle of a.c. supply, SCR2 provides current to the armature winding. In this way, the voltage fed to the motor armature and hence the speed can be controlled.

Q.5. Explain the basic construction & operation of a UJT .

Or

Draw the equivalent circuit of the UJT and discuss its working from the circuit. Draw the characteristics of UJT. Describe some important applications & advantages of UJT.

Related short Questions

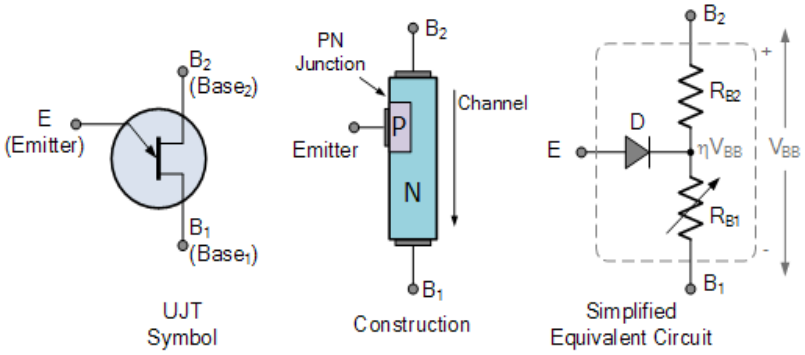
(i) Write short note on construction & working of unijunction transistor [Kanpur 2014]

(ii) Write a short note on unijunction transistor. [Kanpur 2016]

The **Unijunction Transistor** or **UJT** , is a solid state three terminal device used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triacs for AC power control type applications.

Like diodes, unijunction transistors are constructed from separate P-type and N-type semiconductor materials forming a single (hence its name Uni-Junction) PN-junction within the main conducting N-type channel of the device.

Unijunction Transistor has the name of a transistor, its switching characteristics are very different from those of a conventional bipolar or field effect transistor as it can not be used to amplify a signal but instead is used as a ON-OFF switching transistor. UJT's have unidirectional conductivity and negative impedance characteristics acting more like a variable voltage divider during breakdown.



Unijunction Transistor Symbol and Construction

Like N-channel FET's, the UJT consists of a single solid piece of N-type semiconductor material forming the main current carrying channel with its two outer connections marked as Base 2 (B_2) and Base 1 (B_1). The third connection, confusingly marked as the Emitter (E) is located along the channel. The emitter terminal is represented by an arrow pointing from the P-type emitter to the N-type base.

The Emitter rectifying p-n junction of the unijunction transistor is formed by fusing the P-type material into the N-type silicon channel. However, P-channel UJT's with an N-type Emitter terminal are also available but these are little used.

The Emitter junction is positioned along the channel so that it is closer to terminal B_2 than B_1. An arrow is used in the UJT symbol which points towards the base indicating that the Emitter terminal is positive and the silicon bar is negative material. Below shows the symbol, construction, and equivalent circuit of the UJT.

Device Operation

The device has a unique characteristic that when it is triggered, its emitter current increases regeneratively until it is restricted by emitter power supply. It exhibits a negative resistance characteristic and so it can be employed as an oscillator.

The UJT is biased with a positive voltage between n the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes conductivity modulation which reduces the resistance of the portion of the base between the emitter junction and the B_2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits.

Unijunction Transistor Applications

Unijunction transistor circuits were popular in electronics circuits in the 1960s and 1970s because they allowed simple oscillators to be built using just one active device. For example, they were used for relaxation oscillators in variable-rate strobe lights. Later, as integrated circuits became more popular, oscillators such as the 555 timer IC became more commonly used.

In addition to its use as the active device in relaxation oscillators, one of the most important applications of UJTs or PUTs is to trigger thyristors (silicon controlled rectifiers (SCR), TRIAC, etc.). A DC voltage can be used to control a UJT or PUT circuit such that the "on-period"

increases with an increase in the DC control voltage. This application is important for large AC current control.

UJTs can also be used to measure magnetic flux. The hall effect modulates the voltage at the PN junction. This affects the frequency of UJT relaxation oscillators. This only works with UJTs. PUTs do not exhibit this phenomenon.

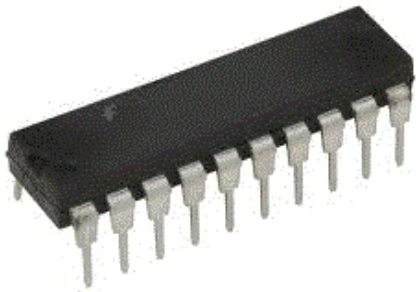
Q.6. What are the integrated circuits ? How they are classified & what are their advantages ?

Related short Questions

(i) Write short note on the basic Linear integrated circuit.
[Kanpur 2015]

(ii) What is an integrated circuit ? Mention its applications
[Kanpur 2015]

An integrated circuit (IC), is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, and transistors are fabricated. IC sometimes called a *chip* or microchip. An IC can function as an amplifier, oscillator, timer, counter, computer memory, or microprocessor. A particular IC is categorized as either linear (analog) or digital, depending on its intended application.



Linear ICs or Analog ICs , such as sensors , power management circuit, and operation amplifiers, Work by processing continuous signals. The most common function they perform are amplification , active filtering, demodulation , mixing , etc.

Digital ICs operate at only a few defined levels or states, rather than over a continuous range of signal amplitudes.These devices are used in computers, computer networks, modems, and frequency counters.The fundamental building blocks of digital ICs are logic gates, which work with binary data, that is,signals that have only two different states, called low (logic 0) and high (logic 1).

Mixed ICs

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D Converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference.

On the fabrication techniques used ICs can be divided into three classes

Monolitic ICs : The word 'monolitic' is derived from the greek monos , meaning 'single' and lithos, meaning 'stone'. Thus monolithic circuit is built into a single stone or single crystal i.e. in monolithic ICs, all circuit components , (both active & passive) and their interconnections are formed into or on the top of a single chip of silicon.

Thin Film ICs

These devices are larger than monolithic ICs but smaller than discrete circuits. These ICs can be used when power requirement is comparatively higher. These ICs are fabricated by depositing films of conducting material on the surface of a glass or ceramic base.

Thick film ICs

These ICs are manufactured by silk-screen printing techniques are used to create the desire circuit pattern on a ceramic substrate.

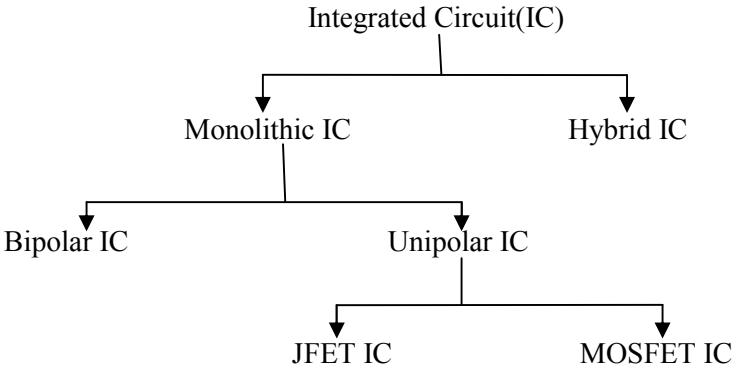
On the basis of chip size the ICs are classified as

SSI i.e. small scale integration having 3-10 gates/chip; MSI i.e. medium scale integration having 30-300 gates/chip; LSI i.e. large scale integration having 300-3,000 gates/chip; VLSI i.e. very large scale integration having more than 3,000 gates/chip.

IC Manufacturing Process

There are two **types of IC** manufacturing technologies one is monolithic technology and other is hybrid technology. In monolithic technique, all electronic component and their interconnections are manufactured together into a single chip of silicon. This technology is applied when identical ICs to be produced in large scale. Monolithic ICs are cheap but reliable.

In hybrid ICs, separate components are attached on a ceramic substance and interconnected by wire or metallization pattern.



Advantages of Integrated Circuits

The major advantages of integrated circuits over those made by interconnecting discrete components are as follows :

1. **Extremely small size** – Thousands times smaller than discrete circuits. It is because of fabrication of various circuit elements in a single chip of semiconductor material.
2. Very small weight owing to miniaturized circuit.
3. Very low cost because of simultaneous production of hundreds of similar circuits on a small semiconductor wafer. Owing to mass production of an IC costs as much as an individual transistor.

4. More reliable because of elimination of soldered joints and need for fewer interconnections.
5. Lower power consumption because of their smaller size.
6. Easy replacement as it is more economical to replace them than to repair them.
7. Increased operating speed because of absence of parasitic capacitance effect.
8. Close matching of components and temperature coefficients because of bulk production in batches.
9. Improved functional performance as more complex circuits can be fabricated for achieving better characteristics.
10. Greater ability of operating at extreme temperatures.
11. Suitable for small signal operation because of no chance of stray electrical pickup as various components of an INC are located very close to each other on a silicon wafer.
12. No component project above the chip surface in an INC as all the components are formed within the chip.

Disadvantages of Integrated Circuits

The major disadvantages of integrated circuits over those made by interconnecting discrete components are as follows :

1. In an IC the various components are part of a small semiconductor chip and the individual component or components cannot be removed or replaced, therefore, if any component in an IC fails, the whole IC has to be replaced by a new one.
2. Limited power rating as it is not possible to manufacture high power (say greater than 10 W) ICs.
3. Need of connecting inductors and transformers exterior to the semiconductor chip as it is not possible to fabricate inductor and transformers on the semiconductor chip surface.
4. Operation at low voltage as ICs function at fairly low voltage.
5. Quite delicate in handling as these cannot withstand rough handling or excessive heat.
6. Need of connecting capacitor exterior to the semiconductor chip as it is neither convenient nor economical to fabricate capacitances exceeding 30pF. Therefore, for higher values of capacitance, discrete components exterior to IC chip are connected.
7. High grade P-N-P assembly is not possible.
8. Low temperature coefficient is difficult to be achieved.
9. Large value of saturation resistance of transistors.
10. Voltage dependence of resistor and capacitors.
11. The diffusion processes and other related procedures used in the fabrication process are not good enough to permit a precise control of the parameter values for the circuit elements. However, control of the ratios is at a sufficiently acceptable level.

Applications of Integrated Circuits

Linear IC's also known as analog Integrated circuits are used in :

1. Power amplifiers
2. Small-signal amplifiers
3. Operational amplifiers
4. Microwave amplifiers
5. RF and IF amplifiers
6. Voltage comparators

7. Multipliers
8. Radio receivers
9. Voltage regulators

Digital IC's are mostly used in computers. They are also referred as switching circuits because their input and output voltages are limited to two levels - high and low i.e. binary. They include:

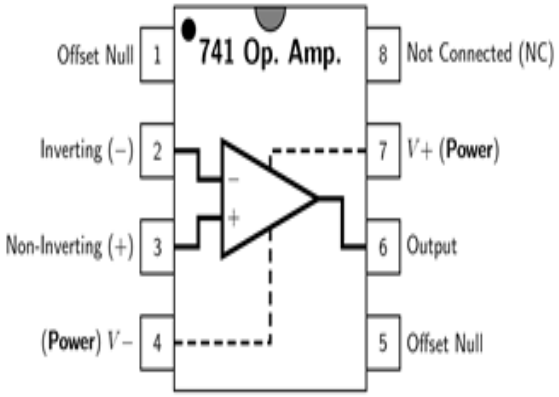
1. Flip-flops
2. Logic gates
3. Timers
4. Counters
5. Multiplexers
6. Calculator chips
7. Memory chips
8. Clock chips
9. Microprocessors
10. Microcontrollers
11. Temperature sensors

Q.7. Discuss the IC related to op amps .

The most commonly used op-amp is IC741. The 741 op-amp is a voltage amplifier, it inverts the input voltage at the output, can be found almost everywhere in electronic circuits.

Pin Configuration:

Let's see the pin configuration and testing of 741 op-amps. Usually, this is a numbered counter clockwise around the chip. It is an 8 pin IC. They provide superior performance in integrator, summing amplifier and general feedback applications. These are high gain op-amp; the voltage on the inverting input can be maintained almost equal to V_{in}.



It is a 8-pin dual-in-line package with a pinout shown above.
Pin 1: Offset null.
Pin 2: Inverting input terminal.
Pin 3: Non-inverting input terminal.
Pin 4: –VCC (negative voltage supply).
Pin 5: Offset null.
Pin 6: Output voltage.
Pin 7: +VCC (positive voltage supply).

Pin 8: No Connection.

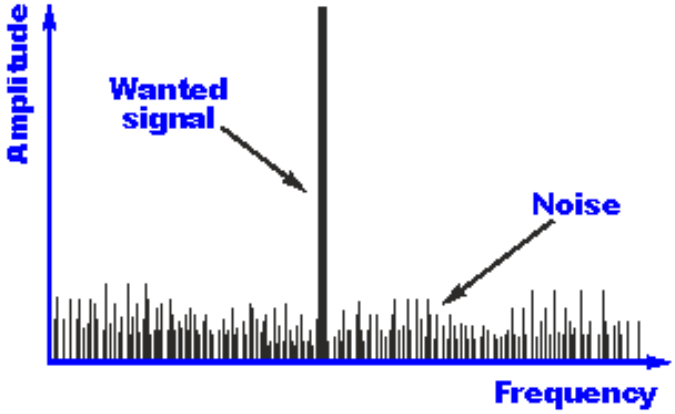
Q.8. What causes 'noise' in electronic circuits ? [Kanpur 2012]

Noise is a random fluctuation in an electrical signal Noise comes in many forms. It can be generated in many ways and noise can affect electronic and radio frequency, RF circuits and systems.

Based on Origin

1. Internal noise
   - Thermal Agitation Noise
   - Shot Noise
   - Transit Time Noise
   - Flicker Noise
   - Miscellaneous Sources

2. External noise
   - Atmospheric
   - Extraterrestrial
     1. Solar
     2. Cosmic
   - Industrial



- ***White noise:*** White noise is the type of noise that affects all frequencies equally. It spreads up from zero frequency upwards with a flat amplitude.
- ***Pink noise:*** Pink noise gains its name from the fact that it does not have a flat response. Its power density falls with increasing frequency. It gains its name because red light is at the lower end of the light spectrum.
- ***Band limited noise:*** Noise can have its frequency band limited either by filters or the circuit through which it passes.

Atmospheric noise (static noise)

This noise is also called static noise and it is the natural source of disturbance caused by lightning discharge in thunderstorm and the natural (electrical) disturbances occurring in nature.

Industrial noise

Sources such as automobiles, aircraft, ignition electric motors and switching gear, High voltage wires and fluorescent lamps cause industrial noise. These noises are produced by the discharge present in all these operations.

Extraterrestrial noise

Noise from outside the Earth includes:

Solar noise

Noise that originates from the Sun is called solar noise. Under normal conditions there is constant radiation from the Sun due to its high temperature. Electrical disturbances such as corona discharges, as well as sunspots can produce additional noise.

Cosmic noise

Distant stars generate noise called cosmic noise. While these stars are too far away to individually affect terrestrial communications systems, their large number leads to appreciable collective effects. Cosmic noise has been observed in a range from 8 MHz to 1.43 GHz.

Energy external of the receiver can couple noise, also by energy conversion. Generally this is done by fundamental interaction, in electronics mainly by inductive coupling and/or capacitive coupling.

Intermodulation noise

Intermodulation noise is caused when signals of different frequencies share the same non-linear medium.

Crosstalk

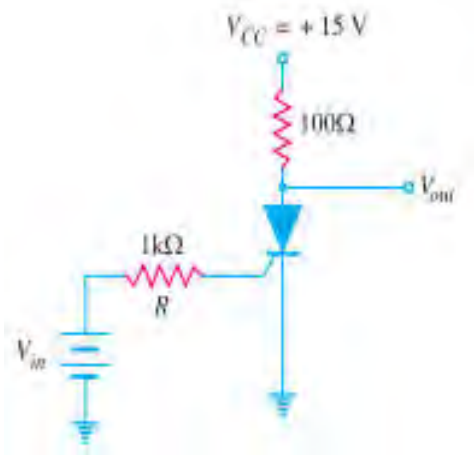
Phenomenon in which a signal transmitted in one circuit or channel of a transmission systems creates undesired interference onto a signal in another channel.

Interference

Modification or disruption of a signal travelling along a medium.

Numerical

Q.1. The SCR of Fig. has gate trigger voltage V_T= 0.7V, gate trigger current I_T= 7 mA and holding current I_H = 6 mA.



(i) What is the output voltage when the SCR is off ?

(ii) What is the input voltage that triggers the SCR ?

(iii) If V_{CC} is decreased until the SCR opens, what is the value of V_{CC} ?

Exp: (i) When SCR is off , there is no current through the 100Ω resistor .

$\therefore V_{out}$= Supply voltage $= V_{CC} = +15V$

(ii) The input voltage V_{in} must overcome $V_T = 0.7V$ also cause 7mA to flow through 1KΩ resistor

$V_{in} = V_T + I_T R$

$\therefore V_{in} = 0.7V + 7mA \times 1k\,\Omega$

$= 7.7V$

(iii) In order to open the SCR , the Vcc must be reduced so that anode current is equal to I_H

Applying KVL to output side we have

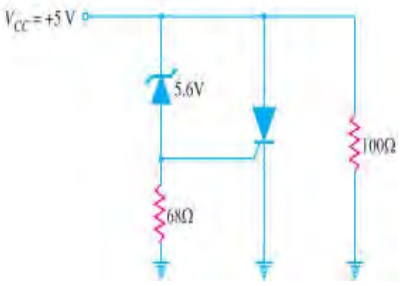
$-V_{CC} + 100\ \Omega \times I_H + V_T = 0$

$V_{CC} = 100\ \Omega \times I_H + V_T$

$\therefore \quad V_{CC} = 100\ \Omega \times 6\ mA + 0.7V$

$= 1.3V$ Ans

Q. 2. In Fig., the SCR has a trigger voltage of 0.7 V. Calculate the supply voltage that turns on the crowbar. Ignore zener diode resistance.

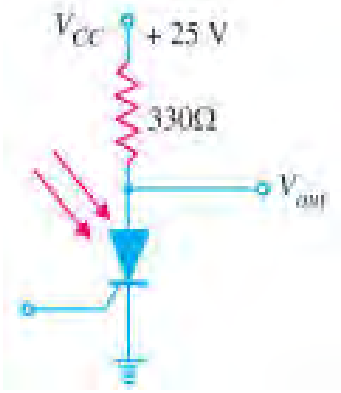


Exp: The breakdown voltage of the zener is 5.6V. To turn on the SCR, the voltage across 68Ωhas to be equal to V_T (= 0.7V)

$\therefore \quad V_{CC} = V_Z + V_T = 5.6 + 0.7 = 6.3V$

When the supply voltage becomes 6.3 V, the zener breaks down and starts conducting. The voltage V_T (= 0.7V) across 68Ω forces the SCR into conduction. When the SCR conducts, the supply voltage is shorted by the SCR and the fuse in the supply voltage burns out. Thus the load (100Ω) is protected from overvoltage.

Q.3. The circuit of Fig. is in a dark room. When a bright light is turned on, the LASCR fires. What is the approximate output voltage? If the bright light is turned off, what is the output voltage?



Exp: Fig. shows a light-activated SCR, also known as a photo-SCR. When light falls on the device, it starts conducting and the output voltage is ideally

$\therefore \quad V_{out} = 0V$

However, if we take into account anode-cathode drop,

$V_{out} = 0.7V.$

When light is turned off, the LASCR stops conducting and the output voltage is equal to the supply voltage V_{CC} i.e.

$V_{out} = V_{CC} = +25V$