Field Effect Transistor

By

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Chapter-7
Field Effect transistor

JFET

The junction FET, abbreviated as JFET has three terminals a source , gate & drain . The JFET has two diodes: the gate-source diode and the gate-drain diode. For normal operation , the gate –source diode is reverse biased; then , the gate voltage controls the drain current.

Drain Curves

Maximum drain current occurs when the gate-source voltage is zero. The pinchoff voltage separates the ohmic and active regions for V_{GS} =0 . The gate-source cutoff voltage has the same magnitude as the pinchoff voltage. $V_{GS(off)}$ turns the JFET off.

Biasing in the Ohmic region

Gate bias is used to bias a JFET in the ohmic region. When it operates in the ohmic region , a JFET is equivalent to a small resistance of R_{DS}. To ensure operation in the ohmic region , the JFET is driven into hard saturation by using V_{GS}= 0 and $I_{D(sat)} << I_{DSS}$

Biasing in the active region

When the gate voltage is much larger than V_{GS}, voltage divider bias can set up a stable Q point in the active region. When +ve & -ve supply voltages are available , two –supply source bias can used to get a stable Q point. Self-bias is used only with small-signal amplifiers because the Q point is less stable than with the other biasing methods.

Transconductance

Transconductance g_m tells us how effective the gate voltage is in controlling the drain current. The quantity g_m is the slope of the transconductance curve, which increases as V_{GS} approaches zero.

The Transconductance curve

This is a graph of drain current versus gate-source voltage. The drain current increases more rapidly as V_{GS} approaches zero. Because the equation for drain current contains a squared quantity, JFETs are referred to as square-law devices. The normalized transconductance curve shows that I_D equals one-quarter of maximum when V_{GS} equal half of cutoff.

JFET Amplifier

A CS amplifier has a voltage gain of $g_m r'_d$ and produces an inverted output signal. One of the most important uses of a JFET amplifier is the source follower, which is often used at the front end of systems because of its high input resistance.

The JFET Analog Switch

JFET acts like a switch that either transmits or blocks a small ac signal. To get this type of action , the JFET is biased into hard saturation or cutoff, depending on whether V_{GS} is high or low. JFET shunt and series switches are used. The series type has a higher on-off ratio.

MOSFET

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a type of field-effect transistor (FET). It has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals.

The D- MOSFET

The depletion mode MOSFET , abbreviated as D- MOSFET is normally on, has a source , gate and drain. The gate is insulated from the channel. Because of this, the input resistance is very high. The D-MOSFET has limited use, mainly in RF circuits.

The E- MOSFET

The Enhancement mode MOSFET is abbreviated as E- MOSFET is normally off. When the gate voltage equals the threshold voltage, an n-type inversion layers connects the source to the drain. When the gate voltage is much greater than the threshold voltage , the device conducts heavily.

MOSFET Preamplifier

MOSFET is an amplifying device in which the output current depends on the input voltage. The MOSFET Pre Amplifier is a sensitive and stable Preamp circuit using an N-Channel MOSFET and a PNP Bipolar transistor. This combination gives high input impedance and low output impedance with stabilized gain.

MOSFET Uses

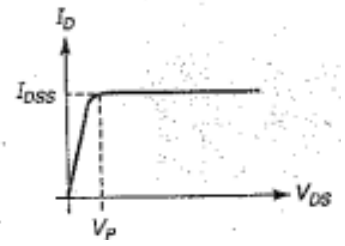
The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices. The MOSFET is very far the most common transistor and can be used in both analog and digital ckt. MOSFET used in various electrical and electronic projects which are designed by using various electrical and electronic components.

CMOS

CMOS uses two complementary MOSFETs, in which one conducts and the other shuts off. The CMOS inverter is a basic digital circuit, CMOS device have the advantage of very low power consumption.

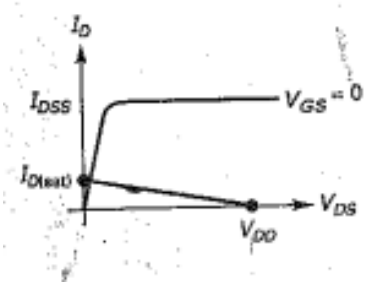
Definitions

Ohmic resistance at pinchoff



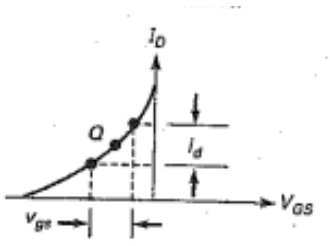
$R_{DS} = V_P / I_{DSS}$

Hard Saturation



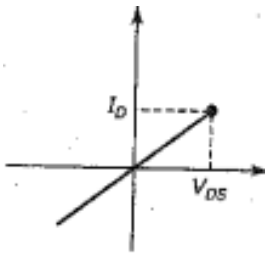
$I_{D(sat)} << I_{DSS}$

Transconductance



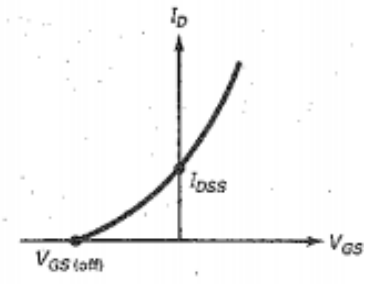
$g_m = i_d / V_{GS}$

Ohmic resistance near origin



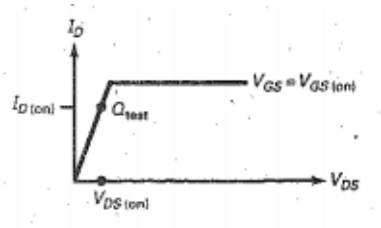
$r_{ds} = V_{DS} / i_D$

D-MOSFET drain current



$I_D = I_{DSS}(1 - V_{GS} / V_{GS(off)})^2$

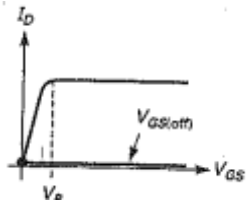
On resistance



$R_{DS(on)} = V_{DS(on)} / I_{D(on)}$

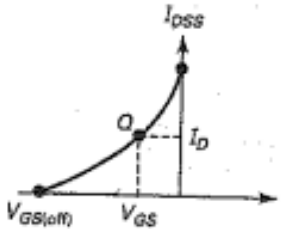
Derivations :

Gate-source cutoff voltage :



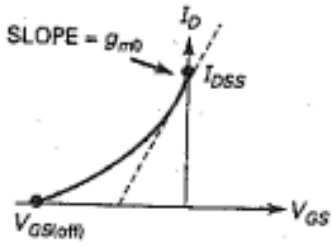
$V_{GS(off)}= -V_P$

Drain current



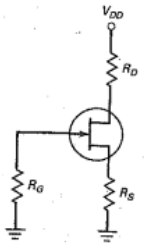
$I_D=I_{DSS}(1-V_{GS}/V_{GS(off)})$

Gate cutoff voltage



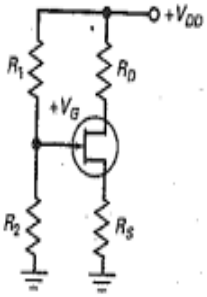
$V_{GS(off)}= -2I_{DSS}/g_{m0}$

Self bias



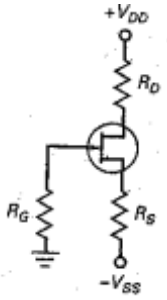
$V_{GS}= -I_DR_S$

Voltage divider bias



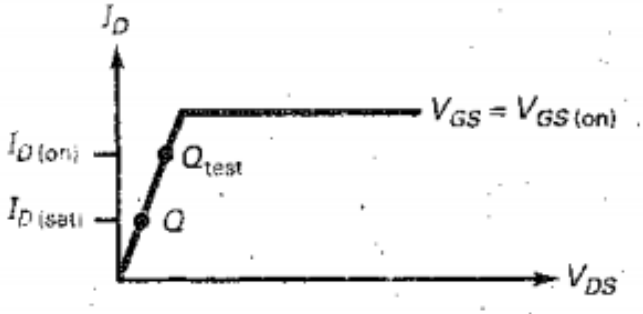
$I_D= (V_G-V_{GS})/R_S \approx V_G /R_S$

Source bias



$I_D = (V_{SS}-V_{GS})/R_S \approx V_{SS} /R_S$

Ohmic region



$I_{D(sat)}< I_{D(on)}$

Long & Short Questions

Q.1. Explain with proper diagram the construction and working of an n-channel JFET. Draw and explain necessary circuit diagram to obtain its characteristics.

Or

With the help of neat sketches and characteristics curve explain the junction FET.

Or

What are the different types of field effect transistor ? Draw drain and output characteristics of a field effect transistor .

Or

Explain pinch-off voltage and draw drain characteristics of FET and also show the parameters of FET and relation between them.

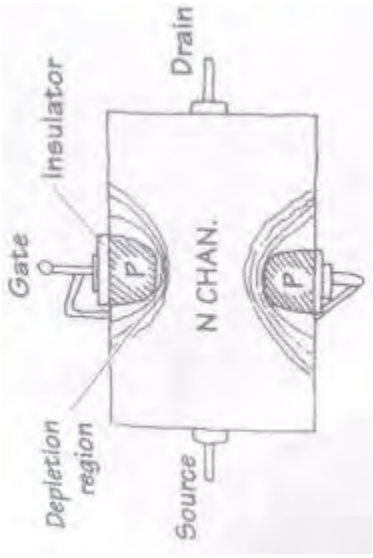
Related Short Answer Questions

(i) Write short note on field effect transistor
(ii) Define the characteristic parameters of a FET and establish the relation between them
(iii) Explain the construction of FET
(iv) Describe the construction of an N-channel JFET

JFET is produced by diffusing two areas of p-type semiconductor into the n-type semiconductor (or two areas of n-type semiconductor into the p-type semiconductor produces p-type JFET) These p- regions are internally connected to get a single external gate lead, the JFET so produced is known as n-channel JFET.

Construction

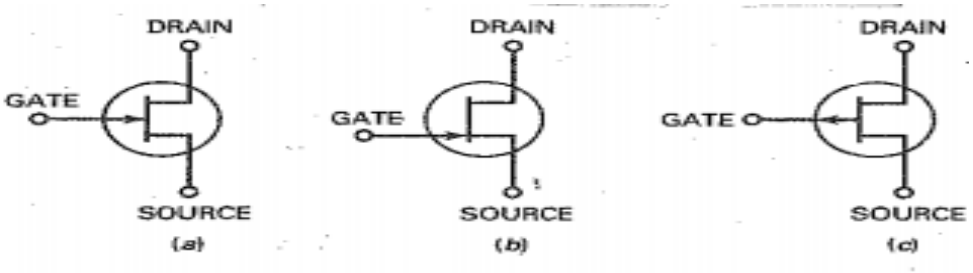
A N- Channel JFET is a JFET whose channel is composed of primarily electrons as the charge carrier. This means that when the transistor is turned on, it is primarily the movement of electrons which constitutes the current flow.
This is in contrast to p-channel JFETs, whose channel is composed primarily of holes, which constitute the current flow.



- A N-Channel JFET is composed of a gate, a source and a drain terminal .It is made with an N-type silicon type silicon channel that contains two P-type silicon terminals placed on either side.
- The gate lead is connected to the p-type terminals, while the drain and source leads are connected to either ends of the N-type channel.

Symbols

Fig.(a) shows schematic symbol of n-channel JFET , fig.(b) shows offset-gate symbol & fig.(c) shows p-channel JFET



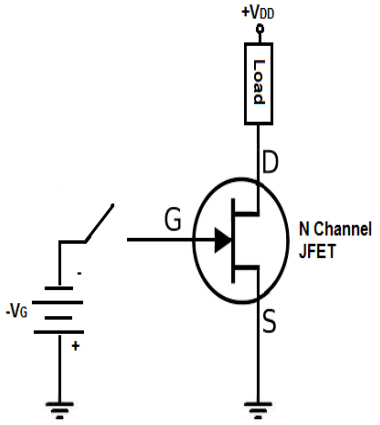
Working

When no voltage is applied to the gate of a N-Channel JFET, current flows freely through the central N-channel. This is why JFETs are referred to as "normally on" devices. Without any applied to the gate terminal of the transistor, they conduct current across from drain-source region.

Typical diagram of voltage biasing of a N- channel JFET is shown in the figure.

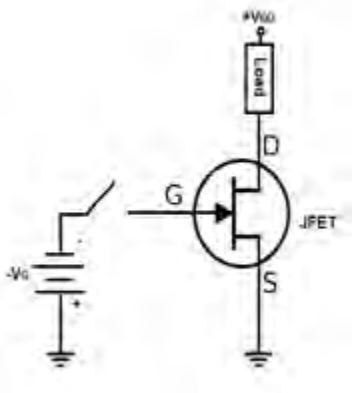
To turn on an N-JFET , + V_{DD} is applied to the drain terminal of the transistor with no voltage applied to the gate terminal of the transistor. This will allow a current to flow through the drain-source channel. If the gate voltage, V_G, is 0V, the drain current is at its largest value for safe operation, and the JFET is in the ON active region.

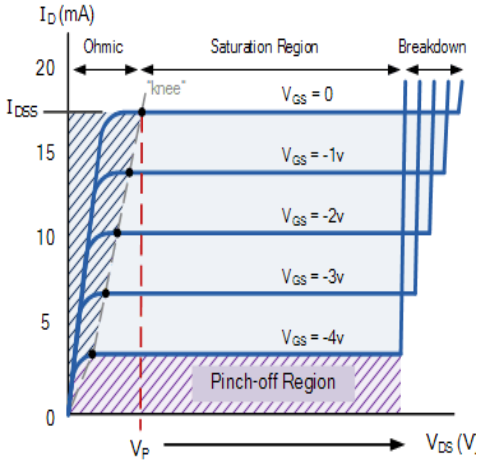
So with a sufficient positive voltage, VDD, and no voltage (0V) applied to the base, the N-channel JFET is in maximum operation and has the largest current.



Voltage biasing of N-channel JFET

Characteristics curve





The voltage V_{GS} applied to the gate controls the current flowing between the drain and the source terminals. V_{GS} refers to the voltage applied between the gate and the source while V_{DS} refers to the voltage applied between the drain and the source.

The characteristics curves shown above, shows the four different regions of operation for a JFET and these are given as:

Ohmic Region : When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

Cut-off Region : This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.

Saturation or Active Region : The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.

Breakdown Region : The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current

Q.2. Describe the action of JFET as a switch in electronic circuits.

When JFET acts as a switch it either transmits or blocks a small signal ac signal. To get this type of action, the gate-source voltage V_{GS} has only two values : either zero or a value that is greater than $V_{GS(off)}$. In this way JFET operates either in the ohmic region or in the cutoff region.

Shunt Switch

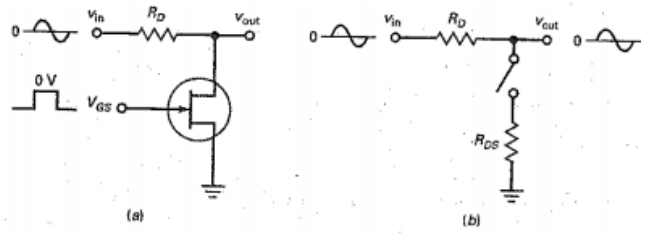


Fig.(a) shows a JFET shunt switch. The JFET is conducting or cut off, depending on whether V_{GS} is high or low.

When V_{GS} is high(0V), the JFET operates in the ohmic region & when V_{GS} is low, the JFET operates in the cutoff as shown in fig.(b).

For normal operation , the ac input voltage must be a small signal, that ensures that the JFET remains in the ohmic region when the ac signal reaches its positive peak. Also R_D is much grater then R_{DS} to ensure hard saturation

$$R_D >> R_{DS}$$

When V_{GS} is high , JFET operates in the ohmic region & the switch is closed therefore $V_{out} = 0V$, when V_{GS} is low, the JFET operates in the cutoff region , so the switch is open. In this case $V_{out} \approx V_{in}$ Therefore , the JFET shunt switch either transmits the ac signal or blocks it.

Series switch

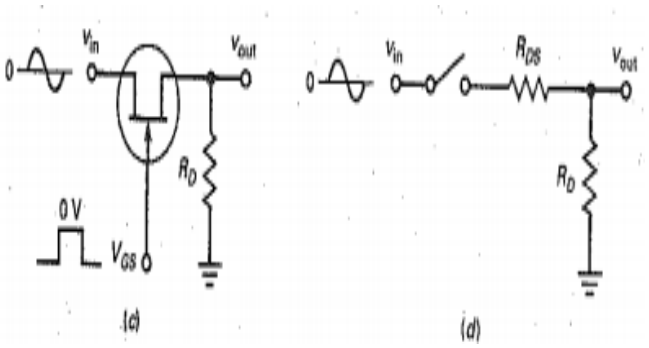
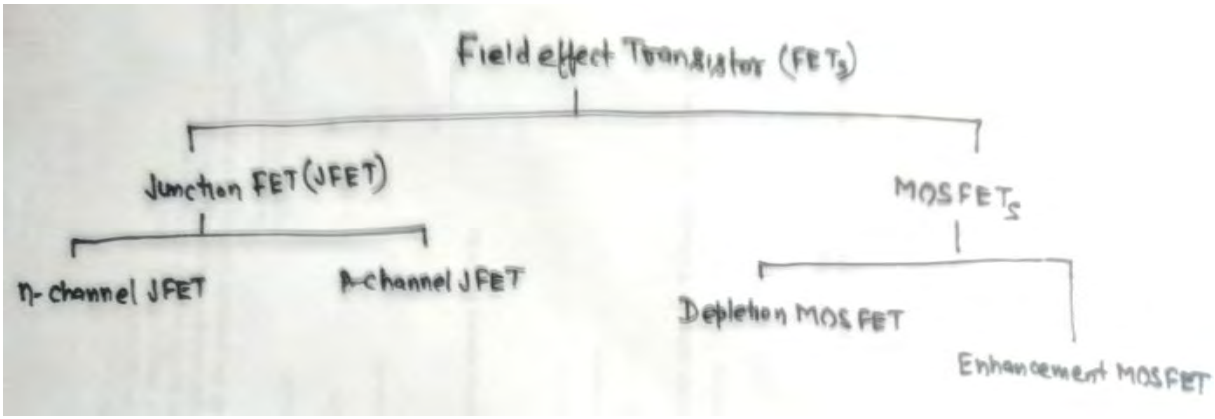


Fig.(c) shows JFET series switch & fig.(d) is equivalent to a resistance of R_{DS}. In this case, the output is approximately equals to input.

When V_{GS} is low , the JFET is open and v_{out} is approximately zero.

When V_{GS} is high i.e. zero , the JFET is close and $V_{out} \approx V_{in}$

Q.3. Explain the classification of Field effect transistor



Q.4. What is the major difference between unipolar & bipolar device?

The basic difference between unipolar & bipolar devices are as below:-

- FET is unipolar device, means the current flowing through it is only due to one type of charge carriers , holes or electrons. BJT on other hand is a bipolar device as holes & electrons both contribute to the flow of current.
- As there is npn & pnp bipolar transistor, there are n-channel & p-channel field effect transistor.
- FET has very high input impedance of megaohms range, which is much higher than the input impedance of BJT.
- FETs are more temperature stable as compare to the BJT and it requires less space than that for a BJT. Therefore FETs are preferred in Integrated circuits.

Q.5. What is MOSFET ? Bring out the difference between MOSFET's and FET's and BJT's.

Related Short Answer Questions

(i) Compare FET with the conventional junction transistor

(ii) What is difference between FET & bipolar transistor ?

Comparison between FET and Junction Transistor

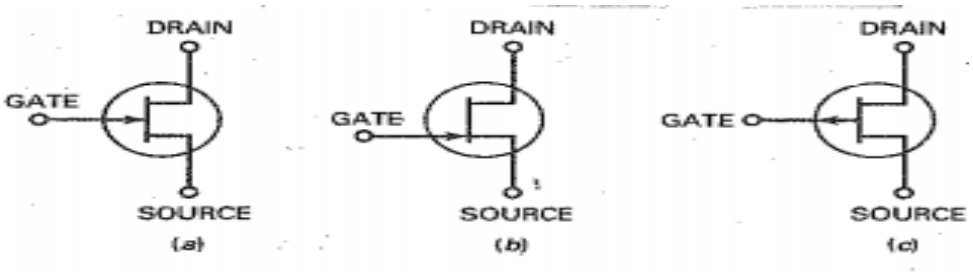
Refer to Q.4.

Comparison between JFET and MOSFET

S.No.	Characteristics	JFET	MOSFET
1	Input Resistance (Ω)	$< 10^9$	$< 10^{12}$
2	Mode of operation	Depletion Mode	Both depletion & Enhancement modes
3	Drain resistance	Higher	Smaller
4	Leakage current	Nearly 10^{-9} A	Nearly 10^{-12} A
5	Output impedance	50kΩ to 1 MΩ	10 kΩ to 50 kΩ
6	Transconductance	1 to 10mAV^{-1}	1 to 10mAV^{-1}

Comparison between NMOS & PMOS

Fig.(a) shows schematic symbol of n-channel JFET , fig.(b) shows offset-gate symbol & fig.(c) shows p-channel JFET



- P-channel is much easier and cheaper to produce compare to N-channel MOSFET device.
- The N-channel MOSFET has high packing density. This makes it faster for switching applications due to smaller junction areas and low inherent capacitances.
- N-channel MOSFET is smaller for same complexity compare to P-channel MOSFET.
- Drain resistance of P-channel MOSFET is 3 times higher than identical N-channel MOSFET device.
- N-channel MOSFET has high false turn-on possibility compare to P-channel device. This is due to positively charged contaminants.
- For given drain current rating, P-channel MOSFET occupies larger area compare to N-channel MOSFET. This is due to the fact that electron mobility is 2.5 times than mobility of hole.

Q.6. What is MOSFET ? Describe the operation of a MOSFET and its types with the help of diagram.

Related Short Answer Questions

(i) Write note on the construction and working of MOSFET.

(ii) Why are N-channel MOSFET preferred over P-channel MOSFET

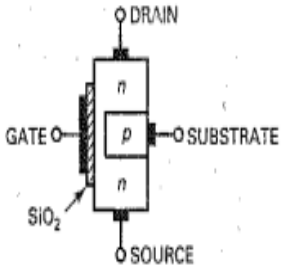
(iii) What do you mean by Enhancement mode of MOSFET

(iv) Explain the representation and working of a depletion mode of a MOSFET.

MOSFET is the metal- oxide semiconductor FET, has a source, gate, and drain. The MOSFET differs from JFET, as in MOSFET gate is insulated from the channel due which gate current is smaller than it is in JFET, that is why MOSFET is also known as IGFET which stands for insulated gate FET .

- There are two kinds of MOSFETs, the depletion- mode typeand the enhancement mode type.
- The enhancement mode MOSFET is widely used in both discrete and integrated circuits. In discrete circuits, the main use is in the power switching, which means turning large currents on and off.
- D-MOSFET are used in high-frequency front-end communication circuits as RF amplifier.

The Depletion –Mode MOSFET



Depletion –Mode MOSFET as shown in figure, a piece of n material with insulated gate on the left and a p region on the right. The p region is called the substrate . Electrons flowing from source to drain must pass through the narrow channel between the gate and the p substrate.

A thin layer of silicon dioxide is deposited on the left side of the channel. In a MOSFET the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when gate voltage is +ve.

Fig. (a) shows a depletion-mode MOSFET with a –ve gate voltage. The V_{DD} supply force free electrons to flow through the narrow channel on the left of the p substrate. As with a JFET , the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller is the drain current. When a gate voltage is negative enough , the drain current cutoff.

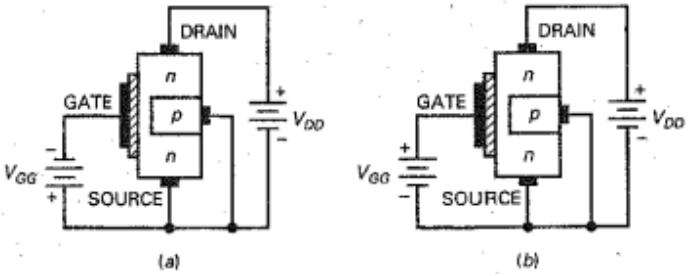
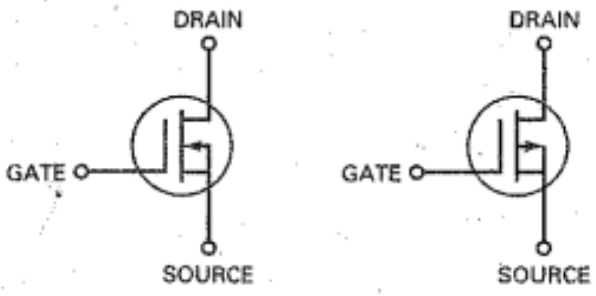


Fig. (b) shows a depletion-mode MOSFET with a + ve gate voltage. The +ve gate voltage increases the number of free electrons flowing through the channel. The more positive the gate voltage, the greater is the conduction from source to drain.

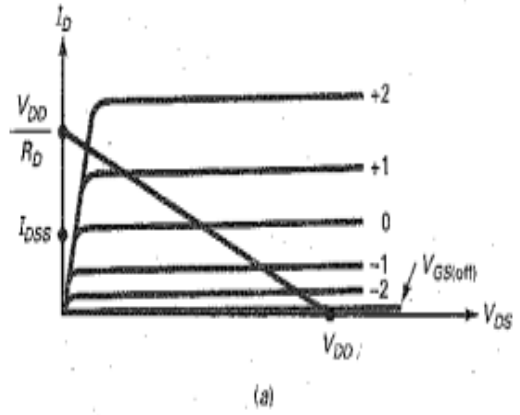
Symbols



n-channel p-channel

D-MOSFET Curves

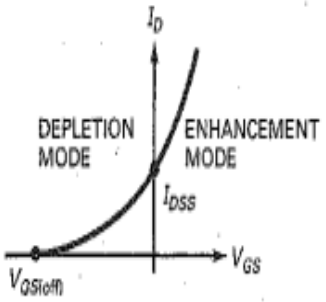
- Fig. (a) shows the set of drain curves for a typical n-channel, depletion –mode MOSFET. The curves above V_{GS}= 0 are positive and the curves below V_{GS}= 0 are negative.
- The bottom curve is for $V_{GS(off)}$ and the drain current will be approximately zero.
- When V_{GS}= 0 , the drain current will be I_{DSS}. This shows that D-MOSFET is a normally on device.
- When V_{GS}< 0 , the drain current is reduced
- When V_{GS} is +ve , I_D will increase following the square-law equation.



(a)

$$I_D=I_{DSS}(1- V_{GS}/ V_{GS(off)})^2$$

- When VG<0 i.e. –ve , the D-MOSFET is operating in the depletion mode. When V_{GS} is +ve , the D-MOSFET is operating in the enhancement mode. Like the JFET, the D-MOSFET curves display an ohmic region, a current source region and a cutoff region.
- Fig.(b) is the transconductance curve for D-MOSFET. I_{DSS} is the drain current with gate shorted to the source.
- The parabolic curve follows the same square-law relation that exits with JFET



(b)

Q.7. Explain the basic operation & output characteristics of n-channel depletion type MOSFET.

Refer to Q.6.

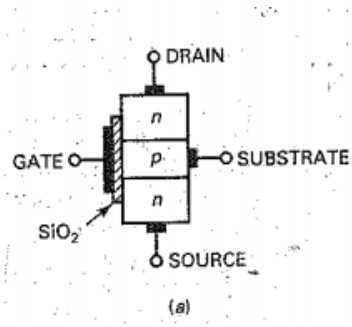
Q.8. Explain with proper diagram, the construction and working of a n-channel e- MOSFET. Draw and explain necessary circuit diagram to obtain it characteristics .

Or

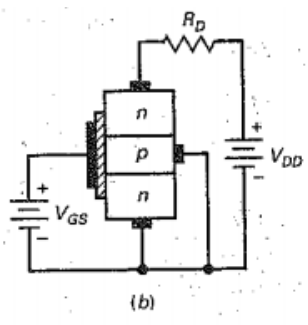
What is enhancement MOSFET ? What do you understand by threshold voltage .

The E-MOSFET as shown in figure(a). The p substrate now extends all the way to the silicon dioxide i.e. there is no longer n channel between the source and the drain.

- Fig. (b) shows normal biasing polarity, when the gate voltage is zero, the current between source and drain is zero, for this reason , an



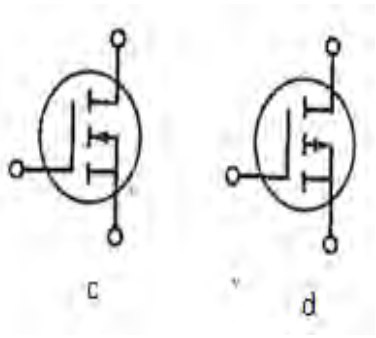
(a)



(b)

E-MOSFET is normally off when the gate voltage is zero.

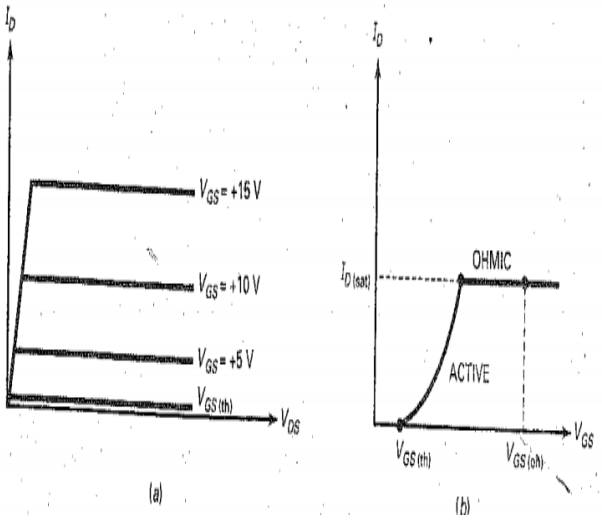
- When the gate voltage is positive, it attracts free electrons into the p region. The free electrons recombines with the holes next to the silicon dioxide.
- When the gate voltage is positive enough, all the holes touching the silicon dioxide are filled and free electrons begin to flow from source to drain.
- The effect is same as creating a thin layer of n-type material next to the silicon dioxide. This thin conducting layer is called the n-type inversion layer. Due to formation of inversion layer electrons can flow easily from the source to the drain.
- The minimum V_{GS} that creates the n-type inversion layer is called the **threshold voltage,** symbolized $V_{GS(th)}$.
- When V_{GS} is less than $V_{GS(th)}$, the drain current is zero. When V_{GS} is greater than $V_{GS(th)}$, an n-type inversion layer connects the source to the drain and the drain current can flow. Typical values of $V_{GS(th)}$ for small-signal devices are from 1 to 3V.
- The schematic symbol is shown in fig. (c) & (d) has a broken channel line indicate this normally off condition.
- The arrow points to inversion layer , which acts like an n channel when the is
- The E-MOSFET is called enhancement because a gate voltage greater than the threshold voltage enhances the conductivity.
- With zero gate voltage, a JFET is on, whereas an E-MOSFET +is off. Therefore, the E-MOSFET is considered to be a normally off device.



Drain Curves

Figure (a) shows a set of drain curves for a typical small-signal E-MOSFET.

- The lowest curve is the $V_{GS(th)}$ curve, when the V_{GS} is lesser then $V_{GS(th)}$, the drain current is approximately zero.
- When the V_{GS} is grater then $V_{GS(th)}$, the device turns on and the drain current is controlled by the gate voltage.
- The almost –vertical part of the graph is the ohmic region, and the almost horizontal part is the active region.
- When biased in the ohmic region , the E-MOSFET is equivalent to a resistor. When biased in the active region , it is equivalent to a current source.



Figure(b) shows a typical transconductance curve .

- There is no drain current until V_{GS}= $V_{GS(th)}$.
- The drain current increases rapidly until it reaches the saturation current $I_{D(Sat).}$
- Beyond $I_{D(Sat)}$, the device is biased in ohmic region
- No change in I_D , even though V_{GS} increases .
- To ensure hard saturation , a gate voltage $V_{GS(on)} > V_{GS(th)}$.

Q.9. Explain how output characteristics of a MOSFET are obtained . Illustrate with proper electronic circuits. Draw output characteristics of depletion type & enhancement type MOSFET and explain the difference between them.

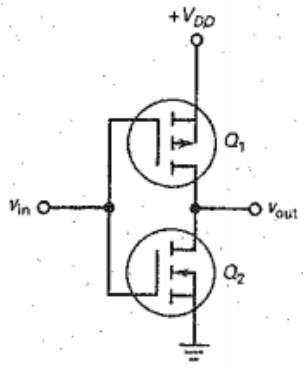
Ref. to Q.6. & Q.8.

Difference between depletion type & enhancement type MOSFET

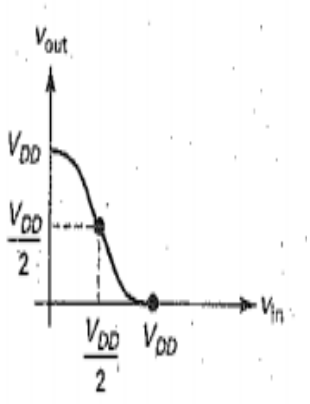
1. Enhancement type mode MOSFET will be off for gate to source voltage 0V as there exists no channel to conduct. Depletion type MOSFET conducts at 0V has positive cut off gate voltage so less preferred. Depletion MOS also conducts at 0V therefore has less useful application.
2. Since the logic operations of depletion MOSFET is the opposite to the enhancement MOSFET, the depletion MOSFET produces positive logic circuits, such as, buffer, AND, and OR.
3. Diffusion current (i.e. sub-threshold leakage current) exists in enhancement MOSFET while depletion MOSFET do not have any diffusion current.
4. As a enhancement MOSFET shrinking in size, there is no way to stop the sub threshold leakage current diffused across from source to drain because the drain and source terminals are closer physically. This is not the problem with depletion type MOSFET because a pinched channel stops the diffusion current completely.
5. Depletion MOSFET logic operations are opposite to enhancement type of MOSFETs.

Q.10. Explain with proper diagram, the construction CMOS. What are the advantages of CMOS over MOSFET ?

CMOS stands for complementary MOSFET as shown in fig. consists of enhancement type n-MOS & p-MOS connected in series with common gate terminal acting as v_{in}.



- The input signal is either $(+V_{DD})$ or (0V). When the input voltage is high Q_1 is OFF & Q_2 is ON.
- In this case , the shorted Q_2 pulls the output voltage down to ground.
- When the input voltage is low Q_1 is ON & Q_2 is OFF.
- In this case , the shorted Q_1 pulls the output voltage up to $+V_{DD}$.
- Since the output voltage is inverted the circuit is called a CMOS inverter.
- For CMOS voltage transfer characteristics i.e. VTC is shown in VTC curve.



VTC curve

Advantages of CMOS

1. Steady state power of CMOS is zero.
2. VTC(voltage transfer characteristics) is nearly ideal i.e. voltage swing is from 0 to V_{DD}.
3. Both NMOS , PMOS acts as load for low and high I/P respectively.
4. Have high FAN IN & FAN OUT.
5. Have high noise margin.

Numerical

Q.1. A JFET has $V_{GS(off)}$ =-4V & I_{DSS}= 5mA. What are the gate voltage & drain current at the half cutoff point ?

Exp: At half cutoff point V_{GS}= -4V/2 = -2V

$\because I_D = I_{DSS}(1- V_{GS}/ V_{GS(off)})^2$

$\therefore I_D = 5mA(1-2/4)^2$

$= 5mA/4 = 1.25mA$ Ans

Q.2. A JFET has I_{DSS}= 5mA and g_{m0}= 500µS. What is the value of $V_{GS(off)}$? What does g_m equal when V_{GS} = -1V ?

Exp: $\because g_{m0} = -2\ I_{DSS}/ V_{GS(off)}$

$\therefore V_{GS(off)} = -2\ I_{DSS}/ g_{m0}$

$\therefore V_{GS(off)} = -2(5mA)/ 500\mu S = -2V$

$\because g_m = g_{m0}\,(1- V_{GS}/ V_{GS(off)})$

$\therefore g_m = (500\ \mu S)\ (1- 1/2)$

$= 2500\ \mu S$ Ans

Q.3. The following readings were obtained in an experiment with FET.

V_{GS}(Volts)	V_{DS}(Volts)	I_D(mA)
0.0	**06**	**12**
0.0	**16**	**12.3**
0.3	**16**	**12.0**

Calculate

(i) AC drain resistance (ii) Transconductance (iii) Amplification Factor

Exp: According to the given reading

For constant V_{GS} at 0V

(i) Change in drain to source voltage (ΔV_{DS}) = 16-6 = 10V

Change in drain Current (ΔI_D) = 12.3-12 = 0.3mA

$\because$ AC drain resistance(r_d) = $\Delta V_{DS} / \Delta I_D$ at constant V_{GS}

$\therefore r_d = 10V/0.3mA = 33.3k\Omega$

(ii) Drain current changes from 12.3mA to 12mA and V_{GS} changes from 0.0V to 0.3V at constant V_{DS} that is at 16V.

ΔV_{GS}= 0.3- 0.0 = 0.3V

ΔI_D = 12.3-12 = 0.3mA

$\because$ Transconductance(g_m) = $\Delta I_D / \Delta V_{GS}$ at constant V_{DS}

$\therefore g_m = 0.3mA / 0.3V = 0.3m$ mho

(iii) Amplification Factor (μ) = $r_d . g_m$

$\therefore \mu = 33.3k\Omega$ x 0.3m mho = 33.3 Ans

Q.2. The following readings were obtained in an experiment with FET.

V_{GS}(Volts)	V_{DS}(Volts)	I_D(mA)
0.0	**7**	**10**
0.0	**15**	**10.25**
-0.2	**15**	**9.65**

Calculate

(i) AC drain resistance (ii) Transconductance

(iii) Amplification Factor of JFET

Exp: According to the given reading

For constant V_{GS} at 0V

(i) Change in drain to source voltage (ΔV_{DS}) = 15-7 = 8V

Change in drain Current (ΔI_D) = 10.25-10 = 0.25mA

$\because$ AC drain resistance(r_d) $= \Delta V_{DS} / \Delta I_D$ at constant V_{GS}

$\therefore r_d = 8V/0.25mA = 32k\Omega$

(ii) Drain current changes from 10.25mA to 9.65mA and V_{GS} changes from 0.0V to -0.2 at constant V_{DS} that is at 15V.

ΔV_{GS}= -0.2- 0.0 = -0.2V

ΔI_D = 9.65-10.25 = -0.6mA

$\because$ Transconductance(g_m) $= \Delta I_D / \Delta V_{GS}$ at constant V_{DS}

$\therefore g_m = -0.6mA / -0.2V = 0.3m$ mho

(iii) Amplification Factor (μ) = $r_d . g_m$

$\therefore \mu = 32k\Omega \times 0.3m$ mho $= 96$ Ans

Q.3. When V_{GS} of a FET changes from -3.1V to -3V the drain current changes from 1mA to 1.3mA. What is the value of transconductance ?

Exp: Given ΔV_{GS}= (-3V)-(-3.1V)= 0.1V

ΔI_D = 1.3mA - 1mA= 0.3mA

$g_m = ?$

$\because$ Transconductance(g_m) $= \Delta I_D / \Delta V_{GS}$

$\therefore g_m = 0.3mA / 0.1V = 3m$ mho Ans

Q.4. When gate- source voltage V_{DS} of a FET changes from -3.1V to -2.9V the drain current changes from 1mA to 1.2mA. What is the value of transconductance ?

Exp: Given ΔV_{GS}= (-2.9V)-(-3.1V)= 0.2V

ΔI_D = 1.2mA - 1mA= 0.2mA

$g_m = ?$

$\because$ Transconductance(g_m) $= \Delta I_D / \Delta V_{GS}$

$\therefore g_m = 0.2mA / 0.2V = 1m$ mho Ans

Q.5. An n-channel FET has I_{DSS} =12mA and pinch off voltage V_P = -4V . Find drain current for V_{GS} = -2V , where symbols have their usual meanings.

Exp: Given I_{DSS} =12mA, V_P = -4V, V_{GS} = -2V , I_D = ?

$\because I_D = I_{DSS}(1 - V_{GS} / V_{GS(off)})^2$

$\therefore I_D = 12mA(1-2/4)^2 = 6mA$ Ans

Q.6. An n-channel silicon JFET has a donor concentration of 2x 10^{21}/ m^3 and a channel width of 4μm , If the dielectric constant of silicon is 12, find the pinch off voltage.

Exp: Given N_D = 2x 10^{21}/ m^3 , Channel width= 4 x10^{-6}m , $k_{silicon}$= 12

V_P(pinch off voltage) =?

$\because V_P = \frac{e\,N_D}{2\epsilon} a^2$,

Putting the values from given data , we have

$\therefore V_P = \frac{e\,N_D}{2k\epsilon_0} a^2$

$\therefore V_P$ = [1.6x 10^{-19} x 2x 10^{21}] x4 x10^{-6}/ [2x 12 x 8.86 x 10^{-12}]

= 6.02volt Ans

Q.7. Sketch the transfer characteristics for an n-channel depletion-type MOSFET with I_{DSS} =10 mA and V_P =-4V.

Exp: At V_{GS}= 0V , I_D= I_{DSS}= 10mA

V_{GS}= V_P = -4V , I_D= 0mA

V_{GS}= V_P /2= -4V /2 = -2V , I_D= 10mA(1-2/4)^2 =2.5mA

At I_D= I_{DSS}/2 , We have V_{GS}= 0.3V_P = -1.2V

Plotting all these points we have transfer characteristics as shown in figure.