Transistor Biasing and Stabilization

By

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Chapter-4
Transistor Biasing and Stabilization

Biasing

We known that transistor can operate i**n a**ny of three regions of operation namely cutoff, active region and saturation. To operate the transistor in these regions the two junction of a transistor should be forward or reversed biased as shown in table

Region of operation	Base Emitter Junction	Collector base junction	Application
Cut off	Reversed bias	Reversed bias	As a switch
Active	Forward bias	Reversed bias	Amplifier
Saturation	Forward bias	Forward bias	As a switch

In order to do so, we need to connect external DC power supplies with correct polarities & magnitude. This process is called as biasing of transistor.

Voltage divider bias (VDB)

The most famous circuit based on the emitter-bias prototype is called voltage divider bias. You can recognize it by the voltage divider in the base circuit.

Accurate VDB Analysis

The Key idea is for the base current to be much smaller than the current through the voltage divider. When the condition is satisfied, the voltage divider holds the base voltage almost constant and equal to the unloaded voltage out of the voltage divider. This Produces a solid Q point under all operating conditions

VDB load line & Q point

The load line is drawn through saturation and cut off. The Q point lies on the load line with the exact location determined by the biasing. Large variations in current gain have almost no effect on the Q point because this type of bias sets up a constant value of emitter current.

Two –Supply emitter bias

This design uses two power supplies: one positive and the other negative . The idea to set up a constant value of „emitter current".

Other types of bias

This section introduced negative feedback, a phenomenon that exits when an increase in an output quantity , produces decreases in an input quantity. It is brillent idea that led to voltage-divider bias. The other type of bias cannot use enough –ve feedback, so they fail to attain the performance level to voltage-divider bias.

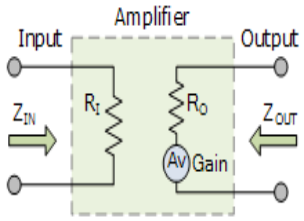
PNP Transistors

These pnp devices have all current & voltages reversed from their npn counterparts. They may be used with negative power supplies; more commonly, they are used with +ve power supplies in an upside-down configuration.

Reverse Feedback ratio

If some percentage of an amplifier"s output signal is connected to the input, so that the amplifier amplifies part of its own output signal, we have what is known as feedback. Feedback comes in two varieties: positive (also called regenerative), and negative (also called degenerative). Positive feedback reinforces the direction of an amplifier"s output voltage change, while negative feedback does just the opposite.

Input & Output impedances



It is the input impedance "seen" by the source driving the input of the amplifier. $\mathbf{Z_{in}}$ or Input Resistance is an important parameter in the design of a transistor amplifier and as such allows amplifiers to be characterized according to their effective input and output impedances as well as their power and current ratings.

For details refer to chapter 3

Bias Stabilization

The stability of a system is a measure of the sensitivity of a network to variations in its parameter. B increases with increase in temperature . Magnitude of V_{BE} decreases about 7.5 mV per degree Celsius (°C) increase in temperature. I_{CO}(reverse saturation current): doubles in value for every 10°C increase in Temperature

Stability Factors, S(I_{CO}), S(V_{BE}), and S(β)

A stability factor,S, is defined for each of the parameters affecting bias stability as listed below:

$$S(I_{CO}) = \Delta I_C / \Delta I_{CO}$$
$$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$$
$$S(\beta) = \Delta I_C / \Delta \beta$$

In each case, the delta symbol signifies change in that quantity.

BJT Transistor modeling

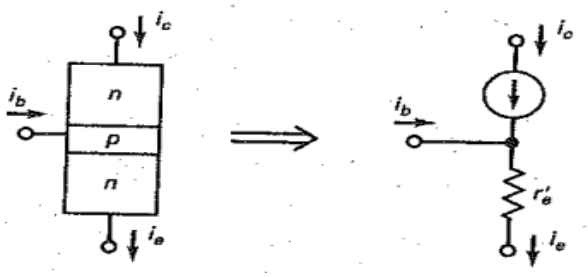
A model is the combination of circuit elements , properly chosen, the best approximates the actual behavior of a semiconductor device under specific operating conditions.

The ac equivalent of a network is

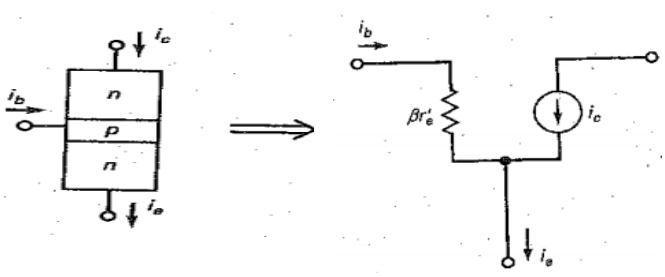
1. Setting all dc sources to zero and replacing them by a short- circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent.
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 & 2.
4. Redrawing the network in a more convenient and logical form.

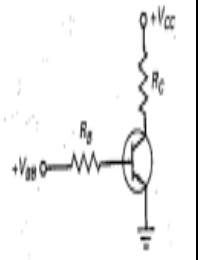
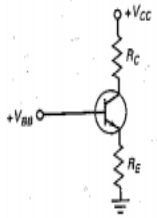
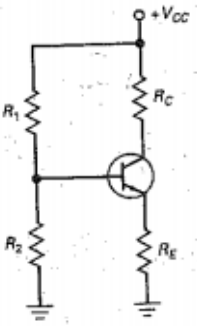
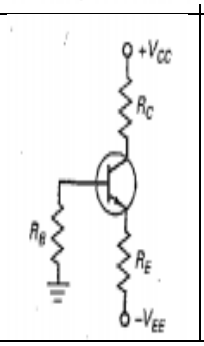
Transistor Model

The T- Model (Ebers- Moll model)



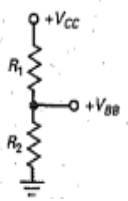
The ɪɪ Model



Type	Circuit	Calculations	Characteristics	Where used
Base bias		$I_B= (V_{BB}-0.7V)/R_B$ $I_C=\beta I_B$ $V_{CE}= V_{CC} - I_C R_C$	Few parts; β dependent; fixed base current	Switch; digital
Emitter bias		$V_E=V_{BB} -0.7V$ $I_E= V_E/ R_E$ $V_C= V_C-I_C R_C$ $V_{CE}=V_C-V_E$	Fixed emitter current; β independent	I_C driver ; amplifier
Voltage divider bias		$V_B=$ $R_2V_{CC}/(R_1+ R_2)$ $V_E= V_B-0.7V$ $I_E= V_E/ R_E$ $V_C= V_{CC}-I_C R_C$ $V_{CE}= V_C - V_E$	Needs more resistors; β independent; needs only one power supply	Amplifier
Two – supply emitter bias		$V_B = 0V$ $V_E= V_B-0.7V$ $V_{RE}=V_{EE}-0.7V$ $I_E=V_{RE}/R_E$ $V_C= V_{CC}- I_C R_C$ $V_{CE}= V_C- V_E$	Needs positive & negative power supplies; β independent;	Amplifier

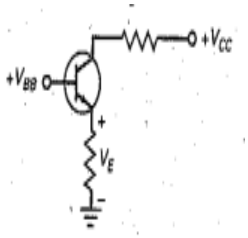
VDB Derivations

Base voltage



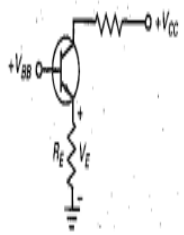
$V_{BB}= R_2V_{CC}/(R_1+ R_2)$

Emitter voltage



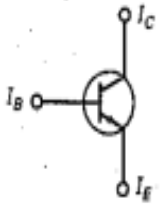
$V_E= V_{BB}- V_{BE}$

Emitter current



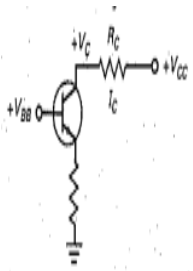
$I_E = V_E / R_E$

Collector current



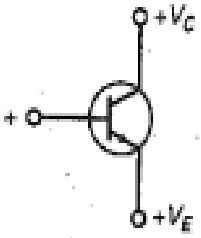
$I_C \approx I_E$

Collector voltage



$V_C = V_{CC} - I_C R_C$

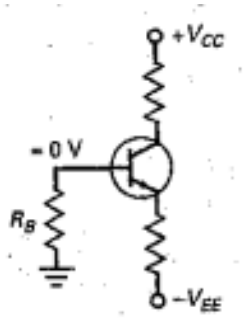
Collector – emitter voltage



$V_{CE} = V_C - V_E$

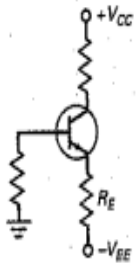
TSEB (Two supply emitter bias) Derivations

Base voltage



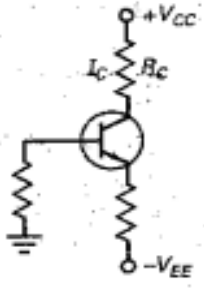
$V_B \approx 0$

Emitter current



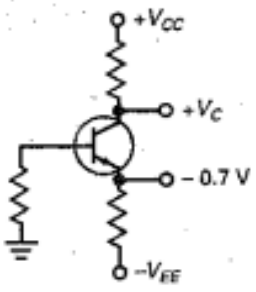
$V_C = V_{CC} - I_C R_C$

Collector Voltage (TSEB)



$V_C = V_{CC} - I_C R_C$

Collector-emitter Voltage (TSEB)



$V_{CE} = V_C + 0.7V$

Long & Short Questions

Q.1. What is meant by transistor –biasing ? Define Stability factor.

Or

What do you understand by transistor by transistor biasing ? Why it is necessary ?

Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

Necessary of transistor biasing

- To active an transistor, biasing is essential. For proper working it is essential to apply to apply voltages of correct polarity across its two junctions.
- If it is not biased correctly it would work inefficiently and produce distortion in the output signal
- Q-point is not middle Output signal is distorted & the signal is clipped
- Further for various applications , BJT is biased as shown in table

Region of operation	Base Emitter Junction	Collector base junction	Application
Cut off	Reversed bias	Reversed bias	As a switch
Active	Forward bias	Reversed bias	Amplifier
Saturation	Forward bias	Forward bias	As a switch

In order to have these applications , we need to connect external DC power supplies with correct polarities & magnitude. This process is called as biasing of transistor.

Stability Factor

The stability of Q point of transistor amplifier depends on the following three parameters :

1. Leakage current I_{CO} 2. β_{dc} 3. Base to emitter voltage

The effect of these parameters can be expressed mathematically by defining the stability factors

1. Stability factor $S = \frac{\Delta I_C}{\Delta I_{CO}} \Big|$ Constant V_{BE} & β_{dc}

   This represents the change in collector current due to change in reverse saturation current I_{CO} The other two parameters that means V_{BE} & β_{dc} are assumed to be constant.

2. Stability factor $S" = \frac{\Delta I_C}{\Delta V_{BE}} \Big|$ Constant I_{CO} & β_{dc}

S‟ represents the change in I_C due to change in V_{BE} at constant I_{CO} & β_{dc}

3. Stability factor $S'' = \frac{\Delta I_C}{\beta dc}\Big|$ Constant I_{CO} & V_{BE}

Total change in collector current

ΔI_C= S. ΔI_{CO} + S‟. ΔV_{BE} + S”. βdc

- Ideally the values of all the stability factors should be zero and practically they should be as small as possible.
- Practically the value of S is significantly higher than the other two stability factor. Hence while comparing the biasing circuits, the values of S is more significant.

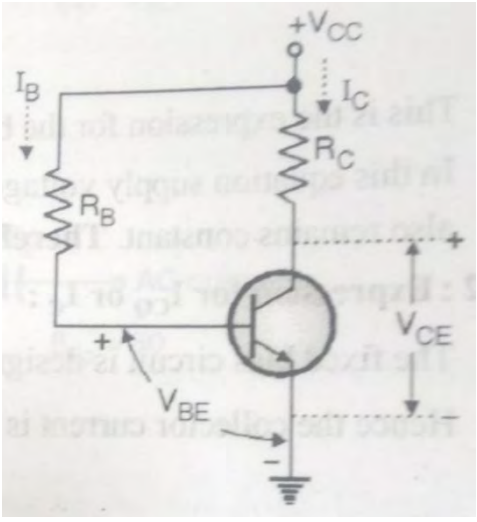
Q.2. What are the various methods used for transistor biasing? Explain one method & State its advantage & disadvantages.

Related Short Answer Questions

(i) What do you mean by biasing of a transistor ? Explain with examples

Biasing is a technique to aid V_{BB} in the input circuit which is separate from the V_{CC} used in the output circuit. The following are the most commonly used method for transistor biasing are as below :

1. Fixed bias circuit (Single base resistor biasing) or base bias
2. Collector to base bias circuit
3. Voltage divider bias circuit (VDB) or self bias
4. Emitter bias or modified fixed bias circuit



Fixed bias circuit (Single base resistor biasing) or base bias

The simplest of all biasing is fixed bias ckt. as shown in fig.

- Before biasing we were using two separate power supplies i.e. V_{CC} & V_{BB} to bias a transistor.
- But in this circuit only one power supply has been used to supply power to both collector as well as base.
- R_B is the single base biasing resistor , hence this circuit is also called as single base resistor biasing.

Analysis of Fixed bias circuit :

As shown in fig. splitting input & output terminals in two loops , namely base circuit & collector circuit

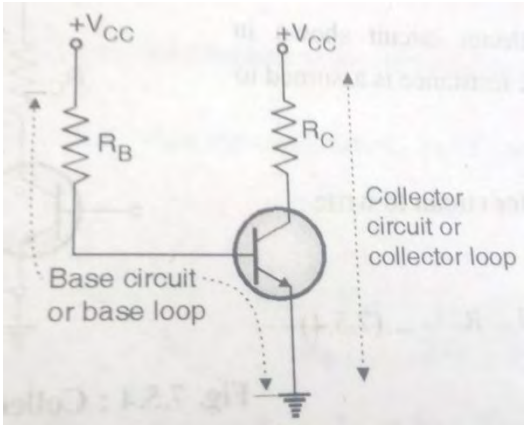


Fig. (a)

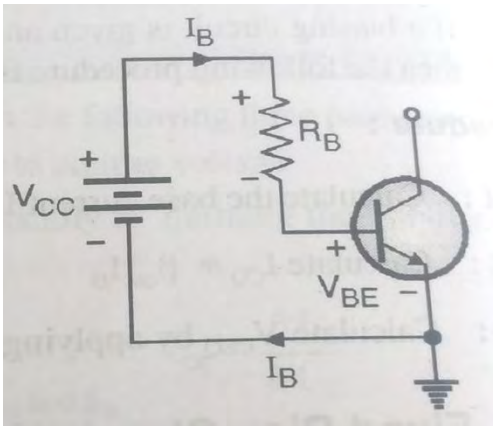


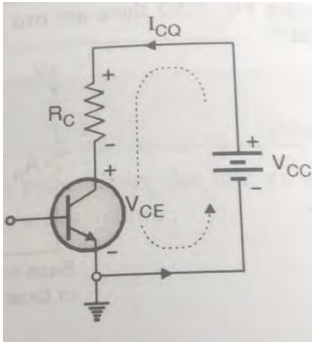
Fig. (b)

as shown in fig.(a).

Expression for I_B

- Consider the base circuit as shown in fig.(b) . Applying KVL to the base circuit we have
  $- V_{CC} + I_B R_B + V_{BE} = 0$
- Rearranging the equation we get
  $I_B = (V_{CC} – V_{BE})/ R_B$
- For silicon V_{BE}= 0.7 and for germanium V_{BE}= 0.3V

Expression for I_C & V_{CE}



Since the fixed bias is operated in the active region therefore

$I_C = \beta I_B + I_{CEO}$

$\because \beta I_B >>> I_{CEO}$

$\therefore I_C = \beta I_B$

Applying KVL to the collector circuit shown , we have

$V_{CC} - I_C R_C – V_{CE} = 0$

$\therefore \quad V_{CE} = V_{CC} - I_C R_C$

Advantages

1. The fixed bias circuit is simple and less number of components.
2. It give very good flexibility as the Q point can be set at any point in the active region by just adjusting the value of R_B .

Disadvantages

1. Vary poor thermal stability as S= 1 + β_{dc}.
2. With changes in β_{dc} due to change in temp. , the operating point keeps on shifting its position.

Q.3. What do you understand by 'Bias stability' of a transistor ? Why is it necessary ? Explain the working of self-bias circuit for common emitter BJT.

Or

Draw the circuit diagram of voltage diagram of voltage divider bias of a transistor . Explain its working.

For definition ref. Q.1

Self Bias

The voltage –divider biasing is known as self bias circuit. The circuit for voltage- divider bias is shown in fig. (a) . The resistance R_1 & R_2 form a potential divider to apply a fixed voltage V_B to the base.

A resistance R_E has been connected in the emitter circuit. This resistance is not present in the fixed bias or collector to base bias circuits.

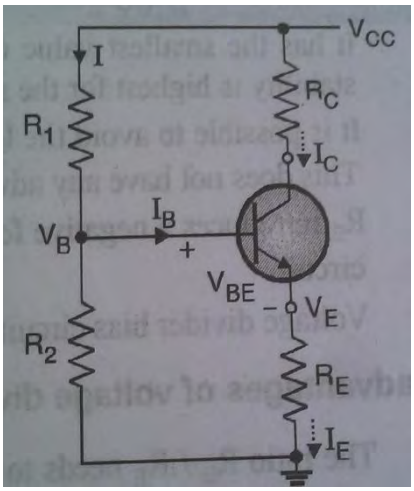


Fig. (a)

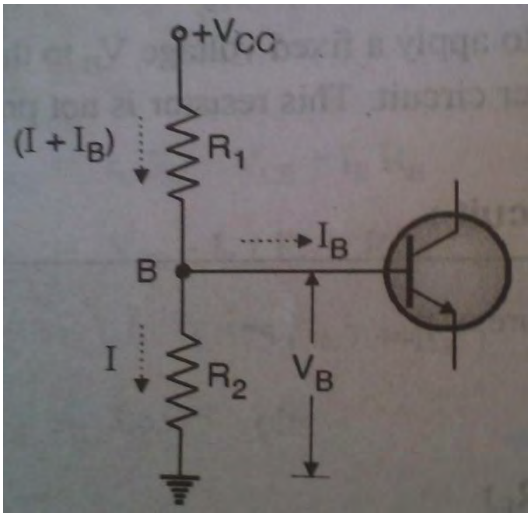


Fig. (b)

Analysis of Voltage divider bias circuit

Base circuit

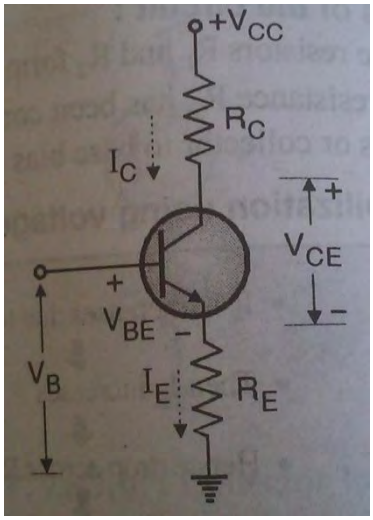
The base circuit as shown in fig(b) . Here we have considered collector & emitter terminals as open circuited . The base Voltage V_B is nothing but the voltage across resistor R_2

i.e. $V_B = \frac{R_2}{R_1+R_2} V_{CC}$

This is because , current through R_1 & R_2 is approx. same and is equal to I.

Collector circuit

The collector circuit as shown in fig., the voltage across emitter resistance R_E can be as follows :



$$V_E = I_E R_E = V_B - V_{BE}$$

$$\therefore \quad I_E = (V_B - V_{BE}) / R_E$$

Applying the KVL to the collector circuit we get

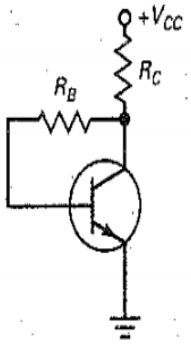
$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$
$$\therefore V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$V_{CE} = V_{CE} - I_E R_E - I_C R_C$$

Bias stabilization

- If I_C increases due to change in temp. or β
- Then I_E increases
- Hence drop across R_E increases ($V_E = I_E R_E$)
- But V_B is constant. Hence V_{BE} decreases.
- Hence I_B decreases.
- Hence I_C also deceases. Thus the compensation for increase in I_C is achived.

Q.4. Draw the circuit diagram of Collector to base bias of a transistor . Explain its working.

Collector to base bias shown in fig. is also known as collector-feedback bias. Historically , this was another attempt at stabilizing the Q point. Again, the basic idea is to feed back a voltage to the base in an attempt to neutralized any change in collector current.



Like emitter-feedback bias circuit , collector feedback bias circuit uses –ve feedback in an attempt to reduce the original change in collector current.

Analysis

Applying KVL in the base circuit we have

$$-V_{CC} + R_C(I_C + I_B) + I_B R_B + V_{BE} = 0$$

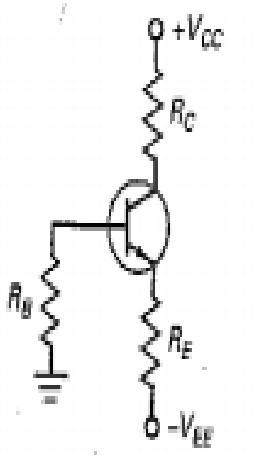
$\because I_B = I_C/\beta$

$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_{C+R_B/\beta}}$

Similarly applying KVL on collector side

We have $V_C = V_{CE} = V_{CC} - I_C R_C$

Q.5. Draw the circuit diagram of two supply emitter bias of a transistor . Explain its working.



Sometimes electronic equipment has a power supply that produces both +ve and –ve supply voltages. The –ve supply forward biases the emitter diode. The +ve supply reverse bias the collector diode.

This circuit is derived from emitter bias, for this reason , we refer to it as two-supply emitter bias (TSEB).

Analysis

$V_B \approx 0$ V

Applying KVL from emitter to base loop in anticlockwise we have

$V_{EE} - I_E R_E - V_{BE} = 0$

$\therefore - I_E = (- V_{EE} + V_{BE}) / R_E = (-V_{EE} + 0.7) / R_E$

$\therefore I_E = (V_{EE} - 0.7) / R_E$

$V(R_E) = V_{EE} - 0.7$ V

Applying KVL on collector side we have

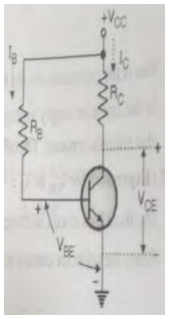
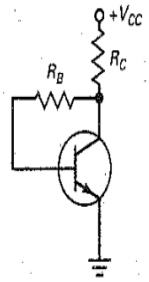
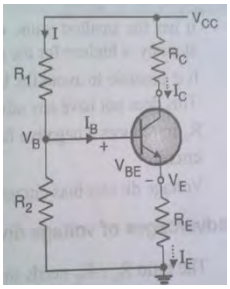
- $V_{CC} + I_C R_C + V_C = 0$

$\therefore V_C = V_{CC} - I_C R_C$

$V_{CE} = V_C - V_E$

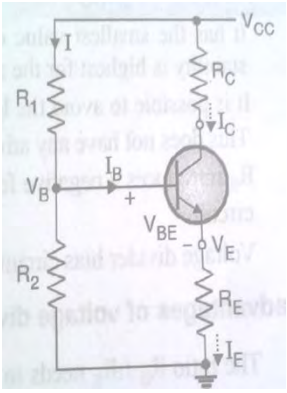
Q.7. Compare Fixed bias, Collector to base bias & Voltage divider bias circuits.

Sr. No.	Parameter	Fixed bias	Collector to base bias	Voltage divider bias
1.	Emitter Resistance	Not used	Not used	Used
2.	-ve Feedback	Not used	Included	Included
3.	Stability	S= (1+ β)	S = (1+ β)/ [1+	S=(1+ β) * [1+ $\frac{R_B}{R_C}$] /

	factor		$\beta(\frac{R_C}{R_{C+}R_B})]$	$[1+\beta+\frac{R_B}{R_C}\ ]$
4.	Q-Point stability	Poor	Moderate	Good
5.	Configuration			

Numerical

Q.1. Determine I_C, V_E, V_B& V_C for the voltage divider configuration .If β=20, R_1= 62KΩ, R_2= 9.1 KΩ , R_C= 3.9 KΩ ,R_E= 0.68 KΩ &V_{CC}= 16V



Exp: As the biasing is voltage divider

We have $V_B = V_{CC}.\ R_2/\ (R_1+R_2)$

$\therefore V_B = 16 \times \frac{9.1k\Omega}{62k\Omega+9.1k\Omega} = 2V$

$\because V_E = V_B - V_{BE}$

$\therefore V_E = 2V - 0.7V = 1.3V$

$\because I_E = V_E / R_E$

$\therefore I_E = 1.3V / 0.68K\Omega = 1.23mA$

$\because I_C = \alpha . I_E = \beta /(\beta+1)\ I_E$

$\therefore I_C = 1.23mA \times 20/21 = 1.17mA$

Q.2. For the fixed bias circuit determine I_B, I_C, V_{CE}, V_B, V_C&V_{BC} for the following parameters R_B = 240 KΩ , R_C= 2.2 KΩ , V_{CC}= 12 V & β=50

Exp: As it is fixed bias

We have $I_B = (V_{CC} - V_{BE})/ R_B$

$\therefore I_B = (12-0.7)/ 240\ K\Omega$

$= 47.08\mu A$

$\because I_C = \beta\ I_B$

$\therefore I_C = 50 \times 47.08\mu A = 2.35mA$

$\because V_{CE} = V_{CC} - I_C R_C$

$\therefore V_{CE} = 12 - 2.35mA \times 2.2\ K\Omega$

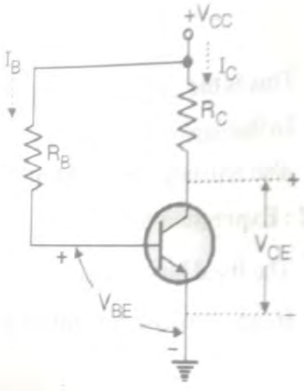
$= 6.83\ V$

$\because$ Emitter terminal is grounded

$\therefore V_B = V_{BE} = 0.7V$

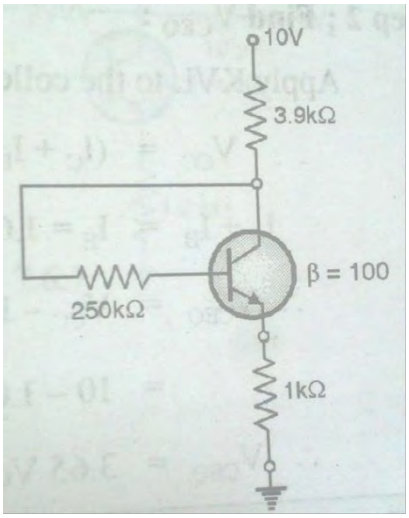
$V_C = V_{CE} = 6.83\ V$

$\because V_{BC} = V_B - V_C$



$\therefore V_{BC} = 0.7V - 6.83V = 6.13\ V$

Q.3. Determine the values of I_C & V_{CE} for the biasing circuit shown in fig.



Exp: As per the given parameters in Collector-emitter feedback

Applying KVL on input side, we have

$-10 + 3.9k\Omega(I_C + I_B) + 250k\Omega.\ I_B + V_{BE} + 1\ k\Omega.\ I_E = 0$

$\because I_E = (1+\beta)I_B$, $I_C = \beta I_B$, $V_{BE}=0.7$ and $\beta = 100$

$\therefore\ -10 + 3.9k\Omega(\beta I_B + I_B) + 250k\Omega.\ I_B + 0.7 + 1\ k\Omega.\ (1+\beta)I_B = 0$

$I_B = 9.3/\ [3.9k\Omega(1+\beta) + 250k\Omega + 1\ k\Omega\ (1+\beta)]$

$I_B = 9.3/\ [3.9k\Omega(1+100) + 250k\Omega + 1\ k\Omega\ (1+100)]$

$I_B = 12.48\ \mu A$ Ans

Q.4. Determine the voltage gain of a single stage CE transistor if the effective resistance of collector circuit is 2kΩ , input resistance is 1kΩ & current gain is 50. [Important]

Exp: Given $R_C = 2k\Omega$, $R_{in} = 1k\Omega$ & $\beta = A_i = 50$

$\because A_V = \beta\frac{R_L}{R_{in}}$

$\therefore A_V = 50 * \frac{2k\Omega}{1k\Omega} = 100$ Ans

Q.5. Determine V_C and V_B for the network of Fig.

Exp: Applying KVL in the anticlockwise for the base-emitter loop , we have

$+V_{EE} - V_{BE} - I_B R_B = 0$

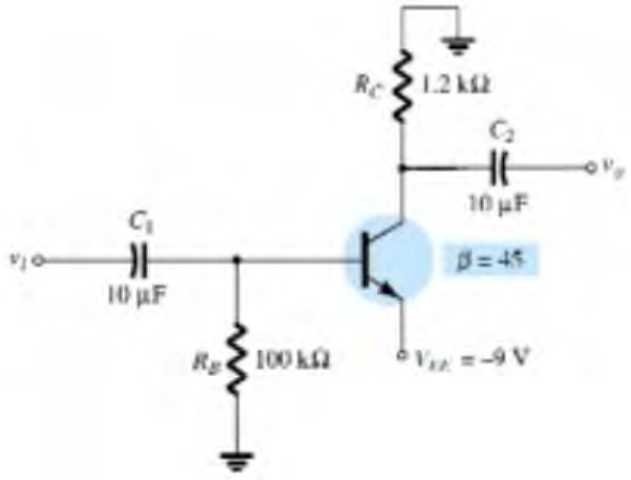
$\therefore I_B = (V_{EE} - V_{BE})/\ R_B$

$\therefore I_B = (9-0.7)/\ 100\ k\Omega = 83\mu A$

$\because I_C = \beta\ I_B$

$\therefore I_C = 45 \times 83\mu A = 3.735\ mA$

$\because V_C = -\ I_C\ R_C$

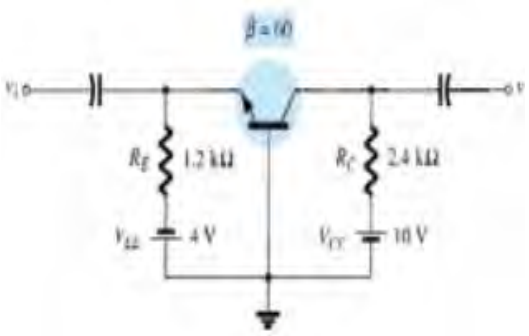


$\therefore V_C = -\ 3.735\ mA \times 1.2\ k\Omega = -4.48\ V$

$\because V_B = -\ I_B\ R_B$

$\therefore V_C = -83mA \times 100\ k\Omega = -8.3\ V$

Q.6. Determine the voltage V_{CB} and the current I_B for the common-base configuration for the given fig.



Exp: Applying KVL to the input circuit yields

$-V_{EE} + I_E R_E + V_{BE} = 0$

$\therefore I_E = (V_{EE} - V_{BE}) / R_E = (4-0.7)/ 1.2k\ \Omega = 2.75mA$

Applying KVL to the output circuit yields

$-V_{CC} + I_C R_C + V_{CB} = 0$

$\therefore V_{CB} = V_{CC} - I_C R_C$

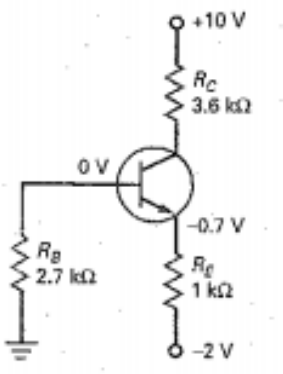
$\because I_C \approx I_E$

$\therefore V_{CB} = 10 - 2.75mA \times 24\ k\ \Omega = 3.4V$

$\because I_B = I_C / \beta$

$\therefore I_B = 2.75mA/ 60 = 45.8\mu A$ Ans

Q.7. What is the collector voltage in the given circuit



Exp: Applying KVL at the Emitter base terminal we have

$+ 2V - 1k\ \Omega \times I_E - V_{BE} = 0$

$\therefore I_E = (\ 2 - 0.7\ ) / 1k\ \Omega = 1.3mA$

$\because V_C = V_{CC} - I_C R_C$

Also $I_C \approx I_E$

$\therefore V_C = 10 - 1.3mA \times 3.6k\ \Omega$

5.32 V Ans